GIGABYTE™

R181-Z90
R181-Z91
R181-Z92

MZ91-FS0 Motherboard for AMD® EPYC™ Series Processors Family

User Manual

Rev. A00

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Documentation Classifications

In order to assist in the use of this product, GIGABYTE provides the following types of documentation:

- User Manual: detailed information & steps about the installation, configuration and use of this product (e.g. motherboard, server barebones), covering hardware and BIOS.
- User Guide: detailed information about the installation & use of an add-on hardware or software component (e.g. BMC firmware, rail-kit) compatible with this product.
- Quick Installation Guide: a short guide with visual diagrams that you can reference easily for installation purposes of this product (e.g. motherboard, server barebones).

Please see the support section of the online product page to check the current availability of these documents.

For More Information

For related product specifications, the latest firmware and software, and other information please visit our website at http://www.gigabyte.com

For GIGABYTE distributors and resellers, additional sales & marketing materials are available from our reseller portal: http://reseller.b2b.gigabyte.com

For further technical assistance, please contact your GIGABYTE representative or visit https://esupport.gigabyte.com/ to create a new support ticket

For any general sales or marketing enquiries, you may also message GIGABYTE server directly by email: server.grp@gigabyte.com

Conventions

The following conventions are used in this user's guide:

	**NOTE!** Gives bits and pieces of additional information related to the current topic.
	**CAUTION!** Gives precautionary measures to avoid possible hardware or software problems.
	**WARNING!** Alerts you to any damage that might result from doing or not doing specific actions.

Server Warnings and Cautions

Before installing a server, be sure that you understand the following warnings and cautions.



WARNING!

To reduce the risk of electric shock or damage to the equipment:

- Do not disable the power cord grounding plug. The grounding plug is an important safety feature.
- Plug the power cord into a grounded (earthed) electrical outlet that is easily accessible at all times.
- Unplug the power cord from the power supply to disconnect power to the equipment.
- Do not route the power cord where it can be walked on or pinched by items placed against it. Pay particular attention to the plug, electrical outlet, and the point where the cord extends from the server.



WARNING!

To reduce the risk of personal injury from hot surfaces, allow the drives and the internal system components to cool before touching them.



WARNING!

This server is equipped with high speed fans. Keep away from hazardous moving fan blades during servicing.



CAUTION!

- Do not operate the server for long periods with the access panel open or removed. Operating the server in this manner results in improper airflow and improper cooling that can lead to thermal damage.
- Danger of explosion if battery is incorrectly replaced.
- Replace only with the same or equivalent type recommended by the manufacturer.
- Dispose of used batteries according to the manufacturer's instructions.

Electrostatic Discharge (ESD)

CAUTION!

ESD CAN DAMAGE DRIVES, BOARDS, AND OTHER PARTS. WE RECOMMEND THAT YOU PERFORM ALL PROCEDURES AT AN ESD WORKSTATION. IF ONE IS NOT AVAILABLE, PROVIDE SOME ESD PROTECTION BY WEARING AN ANTI-STATIC WRIST STRAP ATTACHED TO CHASSIS GROUND -- ANY UNPAINTED METAL SURFACE -- ON YOUR SERVER WHEN HANDLING PARTS.

Always handle boards carefully. They can be extremely sensitive to ESD. Hold boards only by their edges without any component and pin touching. After removing a board from its protective wrapper or from the system, place the board component side up on a grounded, static free surface. Use a conductive foam pad if available but not the board wrapper. Do not slide board over any surface.

System power on/off: To remove power from system, you must remove the system from rack. Make sure the system is removed from the rack before opening the chassis, adding, or removing any non hot-plug components.

Hazardous conditions, devices and cables: Hazardous electrical conditions may be present on power, telephone, and communication cables. Turn off the system and discon-nect the cables attached to the system before servicing it. Otherwise, personal injury or equipment damage can result.

Electrostatic discharge (ESD) and ESD protection: ESD can damage drives, boards, and other parts. We recommend that you perform all procedures in this chapter only at an ESD workstation. If one is not available, provide some ESD protection by wearing an antistatic wrist strap attached to chassis ground (any unpainted metal surface on the server) when handling parts.

ESD and handling boards: Always handle boards carefully. They can be extremely sensi-tive to electrostatic discharge (ESD). Hold boards only by their edges. After removing a board from its protective wrapper or from the system, place the board component side up on a grounded, static free surface. Use a conductive foam pad if available but not the board wrapper. Do not slide board over any surface.

Installing or removing jumpers: A jumper is a small plastic encased conductor that slips over two jumper pins. Some jumpers have a small tab on top that can be gripped with fin-gertips or with a pair of fine needle nosed pliers. If the jumpers do not have such a tab, take care when using needle nosed pliers to remove or install a jumper; grip the narrow sides of the jumper with the pliers, never the wide sides. Gripping the wide sides can dam-age the contacts inside the jumper, causing intermittent problems with the function con-trolled by that jumper. Take care to grip with, but not squeeze, the pliers or other tool used to remove a jumper, or the pins on the board may bend or break.



CAUTION!

Risk of explosion if battery is replaced incorrectly or with an incorrect type. Replace the battery only with the same or equivalent type recommended by the manufacturer. Dispose of used batteries according to the manufacturer's instructions.

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Chapter 1 Hardware Installation

1-1 Installation Precautions

The motherboard/system contain numerous delicate electronic circuits and components which can become damaged as a result of electrostatic discharge (ESD). Prior to installation, carefully read the service guide and follow these procedures:

- Prior to installation, do not remove or break motherboard S/N (Serial Number) sticker or warranty sticker provided by your dealer. These stickers are required for warranty validation.
- Always remove the AC power by unplugging the power cord from the power outlet before installing or removing the motherboard or other hardware components.
- When connecting hardware components to the internal connectors on the motherboard, make sure they are connected tightly and securely.
- When handling the motherboard, avoid touching any metal leads or connectors.
- It is best to wear an electrostatic discharge (ESD) wrist strap when handling electronic components such as a motherboard, CPU or memory. If you do not have an ESD wrist strap, keep your hands dry and first touch a metal object to eliminate static electricity.
- Prior to installing the motherboard, please have it on top of an antistatic pad or within an electrostatic shielding container.
- Before unplugging the power supply cable from the motherboard, make sure the power supply has been turned off.
- Before turning on the power, make sure the power supply voltage has been set according to the local voltage standard.
- Before using the product, please verify that all cables and power connectors of your hardware components are connected.
- To prevent damage to the motherboard, do not allow screws to come in contact with the motherboard circuit or its components.
- Make sure there are no leftover screws or metal components placed on the motherboard or within the computer casing.
- Do not place the computer system on an uneven surface.
- Do not place the computer system in a high-temperature environment.
- Turning on the computer power during the installation process can lead to damage to system components as well as physical harm to the user.
- If you are uncertain about any installation steps or have a problem related to the use of the product, please consult a certified computer technician.

1-2 Product Specifications

CPU	◆ AMD EPYC™ 7002 series processor family ◆ Dual processors, 7nm, Socket SP3 ◆ Up to 64-core, 128 threads per processor ◆ TDP up to 200W Compatible with AMD EPYC™ 7001 series processor family NOTE: If only 1 CPU is installed, some PCIe or memory functions might be unavailable
Chipset	◆ System on Chip
Memory	◆ 32 x DIMM slots ◆ DDR4 memory supported only ◆ 8-Channel memory architecture ◆ RDIMM modules up to 64GB supported ◆ LRDIMM modules up to 128GB supported ◆ Memory speed: Up to 3200*/ 2933 MHz Note: * Follow BIOS setting and memory QVL list if running 3200 Mhz with 2DPC
LAN	◆ 2 x 1GbE LAN ports (1 x Intel® I350-AT2) ◆ 1 x 10/100/1000 management LAN
Expansion Slot	◆ Riser Card CRS1021: ◆ - 2 x PCIe x8 slots (Gen3 x8), Low profile half-length ◆ ◆ Riser Card CRS1015: ◆ - 1 x PCIe x16 slot (Gen3 x16), Low profile half-length ◆ ◆ 2 x OCP mezzanine slots ◆ - PCIe Gen3 x16 ◆ - Type1, P1, P2, P3, P4, K2, K3
Video	◆ Integrated in Aspeed® AST2500 ◆ 2D Video Graphic Adapter with PCIe bus interface ◆ 1920x1200@60Hz 32bpp
Storage (R181-Z90)	◆ 4 x 3.5" hot-swappable HDD bays ◆ 2.5" HDD/SSD supported ◆ SAS card is required for SAS devices support
(R181-Z91)	◆ 2 x 2.5" U.2, 8 x 2.5" SATA/SAS hot-swappable HDD/SSD bays ◆ SAS card is required for SAS devices support
(R181-Z92)	◆ 10 x 2.5" U.2 hot-swappable HDD/SSD bays
SATA	◆ 1 x 7-pin SATA III 6Gb/s with SATA DOM support

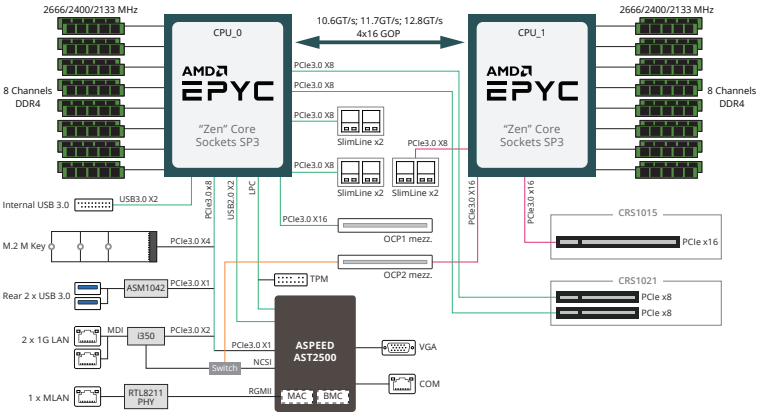
SAS	◆ Supported via add-on SAS Card
Internal Connectors	◆ 1 x 14-pin ATX main power connector ◆ 3 x 4-pin ATX main power connector ◆ 3 x 8-pin ATX 12V power connectors ◆ 1 x 6-pin ATX 12V power connectors ◆ 6 x SlimSAS connectors ◆ 1 x M.2 slot ◆ 2 x CPU fan headers ◆ 1 x USB 3.0 header ◆ 1 x TPM header ◆ 5 x PCIe expansion slots ◆ 2 x OCP mezzanine slots ◆ 2 x Power supply connectors ◆ 1 x Front panel header ◆ 1 x Back plane board header ◆ 1 x PMBus connector ◆ 1 x IPMB connector ◆ 1 x Clear CMOS jumper ◆ 1 x BIOS recovery jumper
Front Panel LED/Buttons	◆ 2 x USB 3.0 ◆ 1 x Power button with LED ◆ 1 x ID button with LED ◆ 1 x NMI button ◆ 1 x Reset button ◆ 2 x LAN activity LEDs ◆ 1 x HDD activity LED ◆ 1 x System status LED
Rear Panel I/O	◆ 2 x USB 3.0 ◆ 1 x VGA ◆ 1 x COM (RJ45 type) ◆ 2 x RJ45 ◆ 1 x MLAN ◆ 1 x ID button with LED
Backplane I/O	◆ Backplane P/N: 9CBP1042NR-00 ◆ Speed and bandwidth: ◆ SAS 12Gb/s, SATA 6Gb/s
TPM	◆ 1 x TPM header with LPC interface ◆ Optional TPM2.0 kit: CTM000

System Management	◆ Aspeed® AST2500 management controller ◆ Avocent® MergePoint IPMI 2.0 web interface: ◆ Network settings ◆ Network security settings ◆ Hardware information ◆ Users control ◆ Services settings ◆ IPMI settings ◆ Sessions control ◆ LDAP settings ◆ Power control ◆ Fan profiles ◆ Voltages, fans and temperatures monitoring ◆ System event log ◆ Events management (platform events, trap settings, email settings) ◆ Serial Over LAN ◆ vKVM & vMedia (HTML5)
Power Supply	◆ 2 x 1200W redundant PSUs ◆ 80 PLUS Platinum ◆ ◆ AC Input: ◆ - 100-240V/ 12-7A, 50-60Hz ◆ - 200-240V/ 7A, 50-60Hz ◆ ◆ DC Output: ◆ - 1200W ◆ - 12V, 80.5A (100-240V) ◆ - 12V, 97A (200-240V) ◆ - 12Vsb, 3A
Environment Ambient Temperature Relative Humidity	◆ Operating temperature: 10°C to 35°C ◆ Non-operating temperature: -40°C to 60°C ◆ Operating humidity: 8-80% (non-condensing) ◆ Non-operating humidity: 20%-95% (non-condensing)
System Dimension	◆ 1U ◆ 438mm (W) x 43.5mm (H) x 730mm (D)

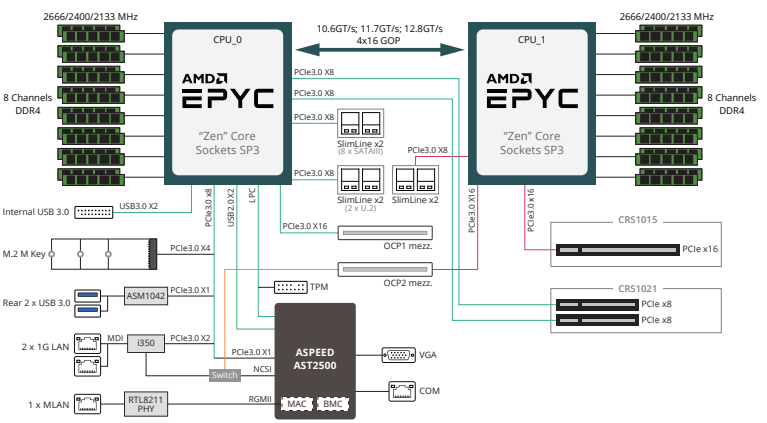
* We reserves the right to make any changes to the product specifications and product-related information without prior notice.

1-3 System Block Diagram

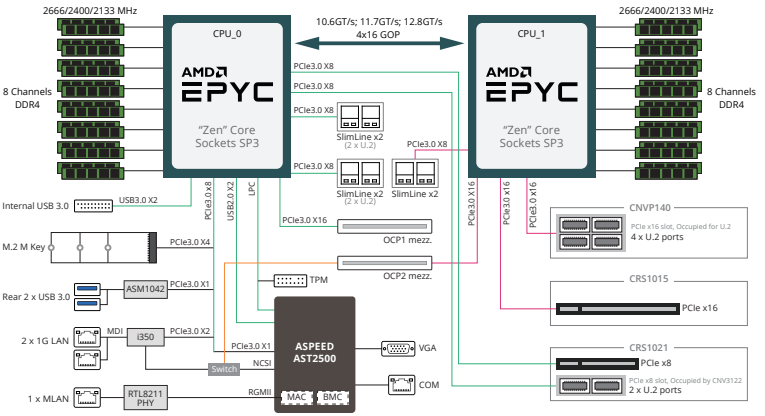
R181-Z90



R181-Z91



R181-Z92


2666/2400/2133 MHz
CPU_0
10.6GT/s; 11.7GT/s; 12.8GT/s
4x16 GOP
CPU_1
2666/2400/2133 MHz
8 Channels DDR4
AMD EPYC
"Zen" Core Sockets SP3
8 Channels DDR4
PCIe3.0 X8
PCIe3.0 X8
PCIe3.0 X8
SlimLine x2 (2 x U.2)
PCIe3.0 X8
PCIe3.0 X8
SlimLine x2 (2 x U.2)
SlimLine x2
Internal USB 3.0
USB3.0 X2
PCIe3.0 x8
USB2.0 X2
LPC
PCIe3.0 X16
OCP1 mezz.
PCIe3.0 X16
PCIe3.0 x16
PCIe3.0 x16
CNVP140
PCIe x16 slot, Occupied for U.2
4 x U.2 ports
M.2 M Key
PCIe3.0 X4
OCP2 mezz.
CRS1015
PCIe x16
Rear 2 x USB 3.0
ASM1042
PCIe3.0 X1
TPM
2 x 1G LAN
MDI
I350
PCIe3.0 X2
PCIe3.0 X1
NCSI
Switch
ASPEED AST2500
VGA
CRS1021
PCIe x8
PCIe x8 slot, Occupied by CNV3122
2 x U.2 ports
1 x MLAN
RTL8211 PHY
RGMII
MAC
BMC
COM

Chapter 2 System Appearance

2-1 Front View

R181-Z90



R181-Z91



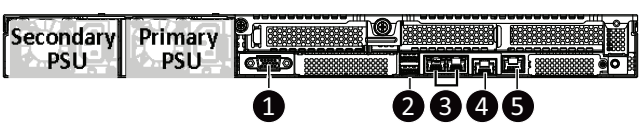
R181-Z92



No.	Description
1.	Front Panel LEDs and buttons
2.	Front USB 3.0 ports
	Orange HDD Latches Support NVMe

- Please Go to Chapter **2-3 Front Panel LED** and Buttons for detail description of function LEDs.

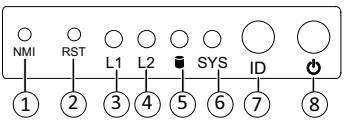
2-2 Rear View



No.	Description
1.	VGA port
2.	USB 3.0 ports
3.	GbE LAN ports
4.	Serial Port
5.	10/100/1000 Server management LAN port

2-3 Front Panel LED and Buttons

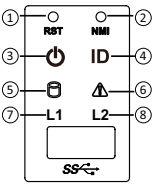
R181-Z90



No.	Name	Color	Status	Description
1.	NMI button			Press the button server generates a NMI to the processor if the multiple-bit ECC errors occur, which effectively halt the server.
2.	Reset Button			Press the button to reset the system.
3/4	LAN 1/2 Active/Link LEDs	Green	Solid On	Link between system and network or no access.
		Green	Blink	Data trasmission or receiving is occuring
		N/A	Off	No data transmission or receiving is occuring
5.	HDD Status LED	Green	On	HDD locate
			Blink	HDD access
		Amber	On	HDD fault
		Green/ Amber	Blink	HDD rebuilding
		N/A	Off	No HDD access or no HDD fault.
6.	System Status LED	Green	Solid On	System is operating normally.
		Amber	Solid On	Critical condition, may indicate: System fan failure System temperature
			Blink	Non-critical condition, may indicate: Redundant power module failure Temperature and voltage issue Chassis intrusion
		N/A	Off	System is not ready, may indicate: POST error NMI error Processor or terminator missing
7.	ID Button			Press the button to activate system identification
8.	Power button with LED	Green	On	System is powered on
		Green	Blink	System is in ACPI S1 state (sleep mode)
		N/A	Off	• System is not powered on or in ACPI S5 state (power off) • System is in ACPI S4 state (hibernate mode)

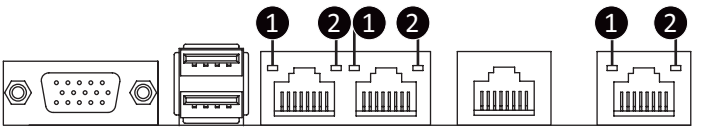
R181-Z91

R181-Z92



No.	Name	Color	Status	Description
1.	Reset Button			Press the button to reset the system.
2.	NMI button			Press the button server generates a NMI to the processor if the multiple-bit ECC errors occur, which effectively halt the server.
3.	Power button with LED	Green	On	System is powered on
		Green	Blink	System is in ACPI S1 state (sleep mode)
		N/A	Off	• System is not powered on or in ACPI S5 state (power off) • System is in ACPI S4 state (hibernate mode)
4.	ID Button			Press the button to activate system identification
5.	HDD Status LED	Green	On	HDD locate
			Blink	HDD access
		Amber	On	HDD fault
		Green/ Amber	Blink	HDD rebuilding
		N/A	Off	No HDD access or no HDD fault.
6.	System Status LED	Green	Solid On	System is operating normally.
		Amber	Solid On	Critical condition, may indicate: System fan failure System temperature
			Blink	Non-critical condition, may indicate: Redundant power module failure Temperature and voltage issue Chassis intrusion
		N/A	Off	System is not ready, may indicate: POST error NMI error Processor or terminator missing
7/8.	LAN 1/2 Active/Link LEDs	Green	Solid On	Link between system and network or no access.
		Green	Blink	Data trasmission or receiving is occuring
		N/A	Off	No data transmission or receiving is occuring

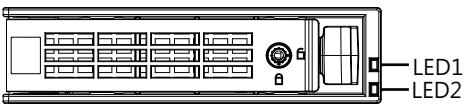
2-4 Rear System LAN LEDs



No.	Name	Color	Status	Description
1.	1GbE Speed LED	Yellow	On	1 Gbps data rate
		Green	On	100 Mbps data rate
		N/A	Off	10 Mbps data rate
2.	1GbE Link/ Activity LED	Green	On	Link between system and network or no access
			Blink	Data transmission or receiving is occurring
		N/A	Off	No data transmission or receiving is occurring

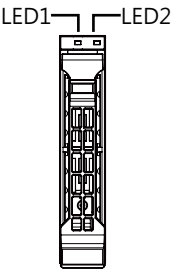
2-5 Hard Disk Drive LEDs

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RAID SKU	LED1	Locate	HDD Fault	Rebuilding	HDD Access	HDD Present (No Access)
No RAID configuration (via HBA, ICH)	Disk LED (LED on Back Panel)	Green	ON(*1)	OFF	Green	OFF
		Amber	OFF	OFF	Amber	OFF
	Removed HDD Slot (LED on Back Panel)	Green	ON(*1)	OFF	Green	--
		Amber	OFF	OFF	Amber	--
RAID configuration (via HW RAID Card or SW RAID Card)	Disk LED	Green	ON	OFF	Alternately	OFF
		Amber	OFF	ON	(Low Speed: 2 Hz)	OFF
	Removed HDD Slot	Green	ON(*1)	OFF	(*3)	--
		Amber	OFF	ON	(*3)	--

LED 2	HDD Present	No HDD
Green	ON	OFF

NOTE:

*1: Depends on HBA/Utility Spec.

*2: Blink cycle depends on HDD's activity signal.

*3: If HDD is pulled out during rebuilding, the disk status of this HDD is regarded as faulty.

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Chapter 3 System Hardware Installation



Pre-installation Instructions

Computer components and electronic circuit boards can be damaged by discharges of static electricity. Working on computers that are still connected to a power supply can be extremely dangerous. Follow the simple guidelines below to avoid damage to your computer or injury to yourself.

- Always disconnect the computer from the power outlet whenever you are working inside the computer case.
- If possible, wear a grounded wrist strap when you are working inside the computer case. Alternatively, discharge any static electricity by touching the bare metal system of the computer case, or the bare metal body of any other grounded appliance.
- Hold electronic circuit boards by the edges only. Do not touch the components on the board unless it is necessary to do so. Do not flex or stress the circuit board.
- Leave all components inside the static-proof packaging until you are ready to use the component for the installation.

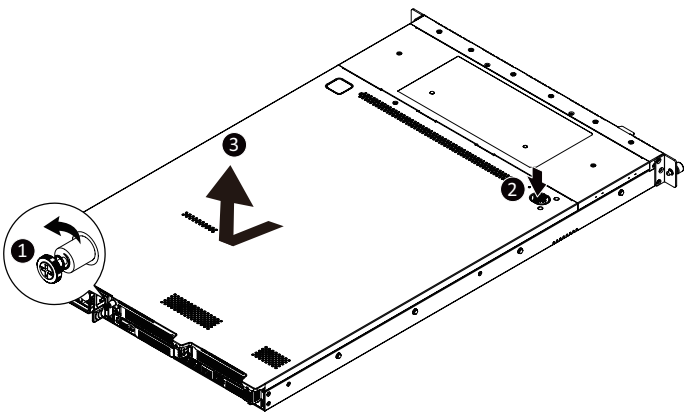
3-1 Removing Chassis Cover

Before you remove or install the system cover

- Make sure the system is not turned on or connected to AC power.

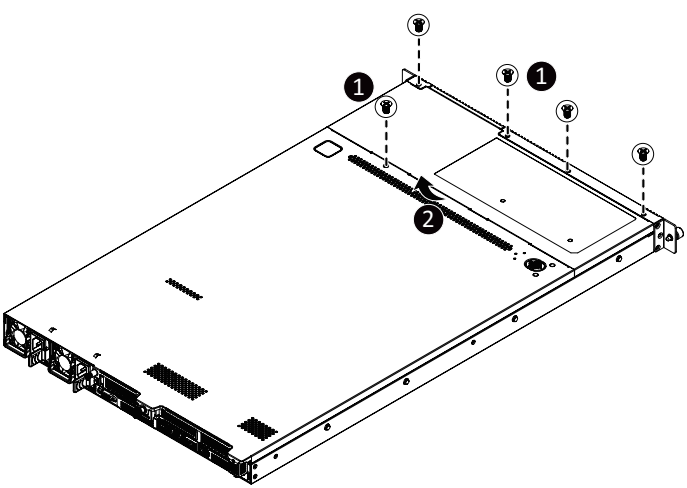
Follow these instructions to remove the rear system cover:

1. Loosen and remove the thumbscrew securing the back cover.
2. Push down the indentation located at the side of the back chassis
3. Slide the cover horizontally to the back and remove the cover in the direction of the arrow.



Follow these instructions to remove the front system cover:

1. Remove the five screws securing the front system cover to the system.
2. Flip open the front system cover.

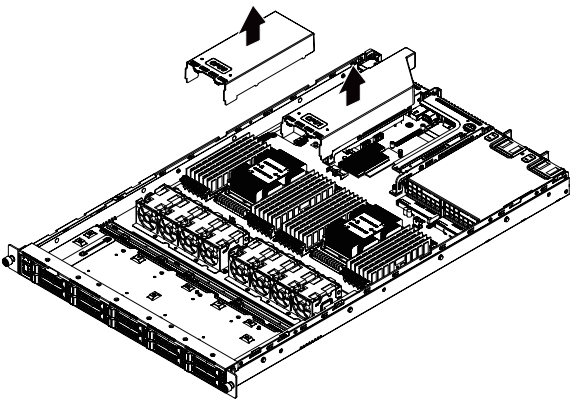


3-2 Removing and Installing the Fan Duct

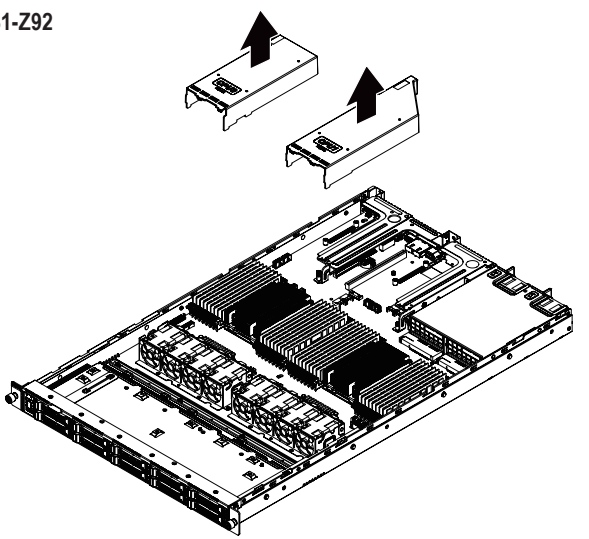
Follow these instructions to remove/install the fan duct:

1. Lift up to remove the two fan ducts
2. To install the fan duct, align the fan duct with the guiding groove. Push down the fan duct into chassis until its firmly seats

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3-3 Installing the CPU and Heat Sink

Read the following guidelines before you begin to install the CPU:

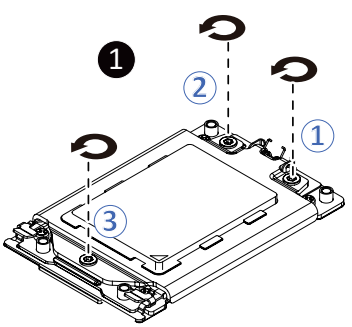
- •Make sure that the motherboard supports the CPU.
- •Always turn off the computer and unplug the power cord from the power outlet before installing the CPU to prevent hardware damage.
- •Unplug all cables from the power outlets.
- •Disconnect all telecommunication cables from their ports.
- •Place the system unit on a flat and stable surface.
- •Open the system according to the instructions.

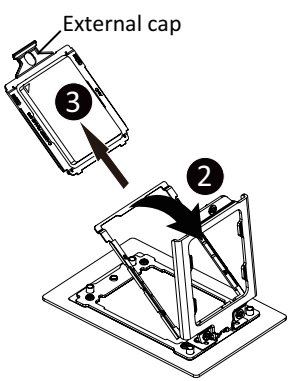
WARNING!

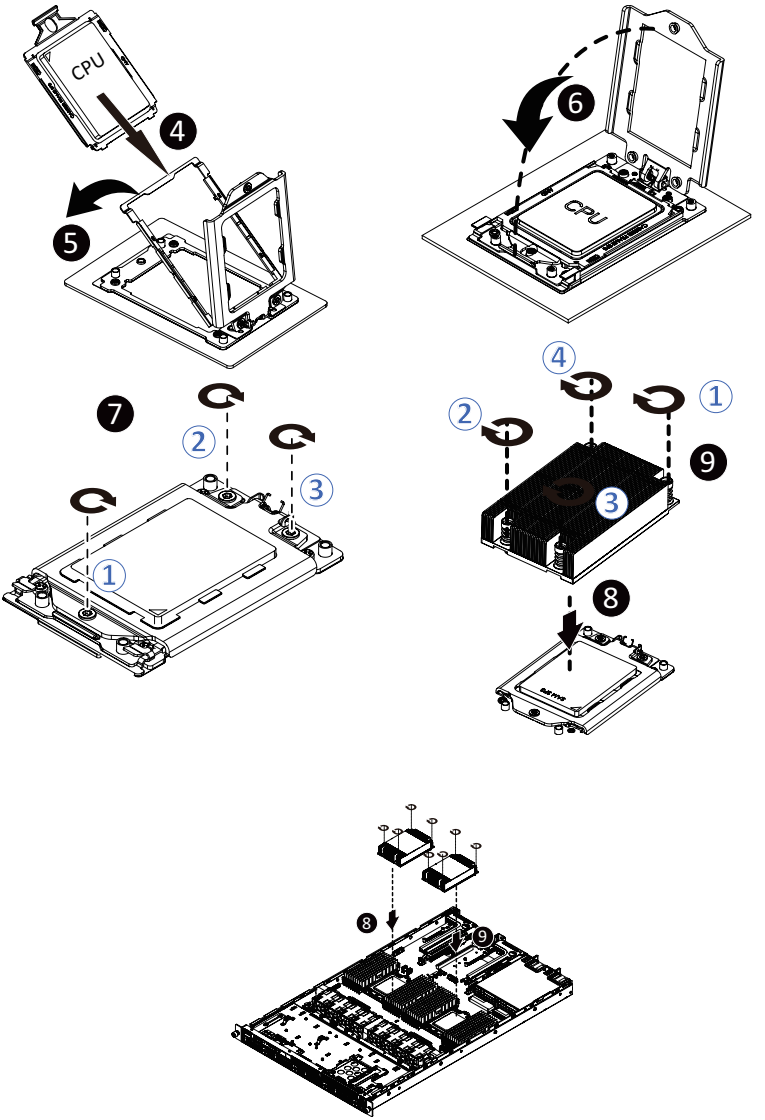
Failure to properly turn off the server before you start installing components may cause serious damage. Do not attempt the procedures described in the following sections unless you are a qualified service technician.

Follow these instructions to install the CPU:

1. Align and install the processor on the carrier, making sure to line up the triangle markers on the corner of the CPU to the triangle mark on the corner of the CPU carrier.
2. Slide the carrier assembly into the channels of the carrier bracket
3. Close the carrier bracket so that it firmly latches on to the CPU socket.
4. Close the CPU socket cover.
5. Tighten and secure the CPU socket cover screws in the following order (3→2→1).
   NOTE: When removing the CPU socket cover, loosen the screws in reverse order (1→2→3).
   NOTE: Apply thermal compound evenly on the top of the CPU. Remove the protective cover from the underside of the heat sink.
6. Align and place the heatsink onto the top of the CPU socket.
7. To secure the heatsink, tighten the four screws to the CPU socket.
8. Repeat steps 1-7 for the second CPU and heatsink.
9. To remove the heatsinks and CPUs, follow steps 1-7 in reverse order.






CPU
4
5
6
CPU
7
2
3
1
4
2
1
9
3
8
8
9

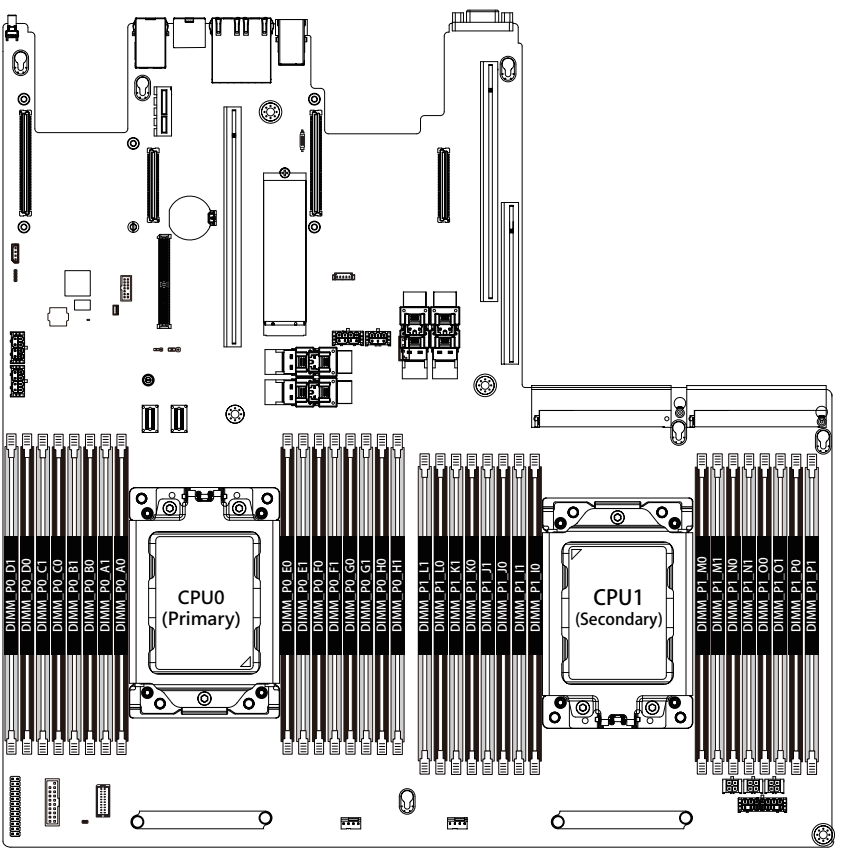
3-4 Installing the Memory

Read the following guidelines before you begin to install the memory:

- Make sure that the motherboard supports the memory. It is recommended that memory of the same capacity, brand, speed, and chips be used.
- Always turn off the computer and unplug the power cord from the power outlet before installing the memory to prevent hardware damage.
- Memory modules have a foolproof design. A memory module can be installed in only one direction. If you are unable to insert the memory, switch the direction.

3-4-1 Eight Channel Memory Configuration

This motherboard provides 32 DDR4 memory sockets and supports Eight Channel Technology. After the memory is installed, the BIOS will automatically detect the specifications and capacity of the memory. Enabling Four Channel memory mode will be four times of the original memory bandwidth.



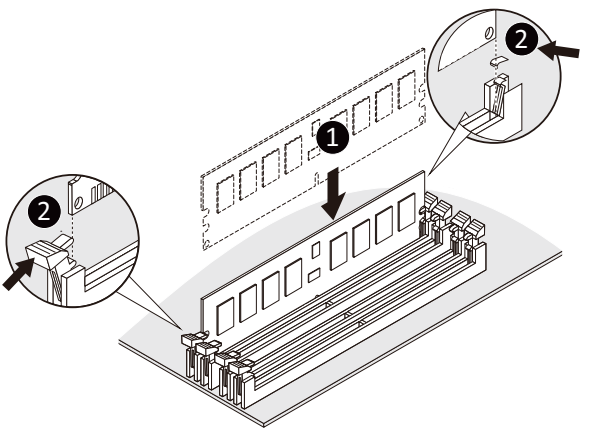
3-4-2 Installing a Memory

Before installing a memory module, make sure to turn off the computer and unplug the power cord from the power outlet to prevent damage to the memory module.

Be sure to install DDR4 DIMMs on this motherboard.

Follow these instructions to install the Memory:

1. Insert the DIMM memory module vertically into the DIMM slot, and push it down.
2. Close the plastic clip at both edges of the DIMM slots to lock the DIMM module.
3. Reverse the installation steps when you want to remove the DIMM module.



3-4-3 DIMM Population Table

RDIMM Maximum Frequency Supported Tablel

DIMMs Populated	DIMM		Frequency (MT/s)
	1R	2R 2DR	1.2V
1	1	--	3200
	--	1	3200
2	2	--	2933
	1	1	2933
	--	2	2933

LRDIMM Maximum Frequency Supported Table

DIMMs Populated	DIMM		Frequency (MT/s)
	2S2R 2S4R	4DR	1.2V
1	1	--	3200
	--	1	3200
2	2	--	2933
	1	1	Not Supported
	--	2	2933

3DS RDIMM Maximum Frequency Supported Table

DIMMs Populated	DIMM	Frequency (MT/s)
	2S2R 2S4R	1.2V
1	1	2933
2	2	2666

NOTE!

- 1R: 1 package rank of SDP DRAMs
- 2R: 2 package rank of SDP DRAMs
- 2DR: 2 package rank of DDP DRAMs
- 4DR: 4 package rank of DDP DRAMs
- 2S2R/2S4R/2S8R: 2 package rank of 2/4/8 high 3DS DRAMs
- DIMM must be populated in sequential alphabetic order, starting with bank A.
- When only one DIMM is used, it must be populated in memory slot A1.

3-5 Installing the PCI Expansion Card

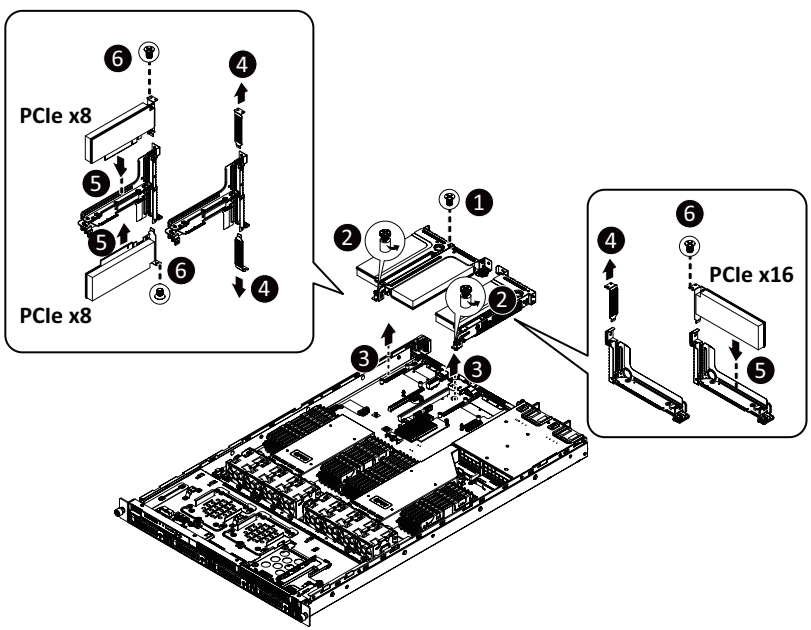
- Voltages can be present within the server whenever an AC power source is connected. This voltage is present even when the main power switch is in the off position. Ensure that the system is powered-down and all power sources have been disconnected from the server prior to installing a PCI card.

Failure to observe these warnings could result in personal injury or damage to equipment.

- The PCI riser assembly does not include a riser card or any cabling as standard. To install a PCI card, a riser card must be installed.

Follow these instructions to PCI Expansion card:

1. Remove the securing special screw on the riser bracket.
2. Remove the thumbscrew on the riser bracket
3. Lift up the riser bracket out of system.
4. Remove the slot covers from the riser bracket.
5. Orient the PCI-E card with the riser guide slot and push in the direction of the arrow until the PCI-E card sits in the PCI card connector.
6. Secure the PCI-E card with the screw.
7. Reverse the steps 3 - 1 to install the riser bracket.



3-6 Installing the Hard Disk Drive

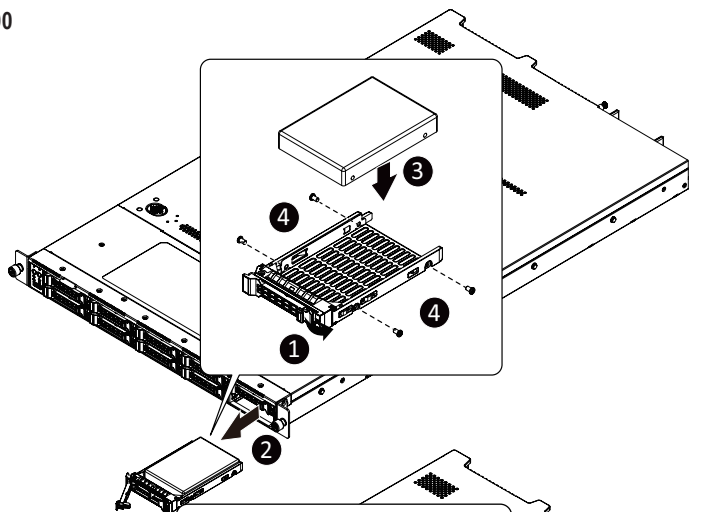
Read the following guidelines before you begin to install the Hard disk drive:

- Take note of the drive tray orientation before sliding it out.
- The tray will not fit back into the bay if inserted incorrectly.
- Make sure that the HDD is connected to the HDD connector on the backplane.

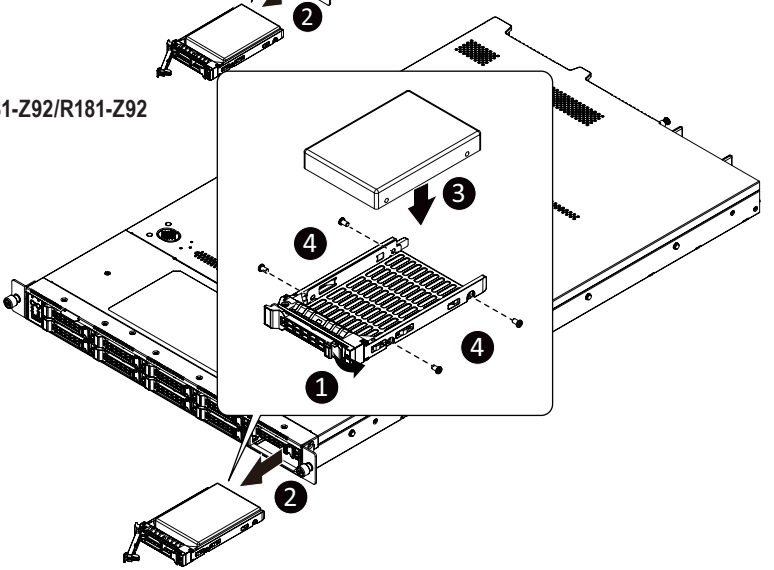
Follow these instructions to install a 3.5" hard disk drive:

1. Press the release button.
2. Extend the locking lever and pull the locking lever to remove the HDD tray.
3. Place the hard disk drive into the HDD tray.
4. Secure the hard disk drive to the HDD tray with four screws.

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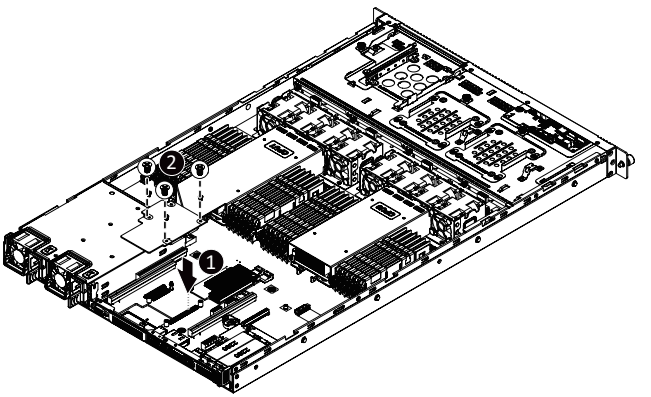


3-7 Installing the Mezzanine Card

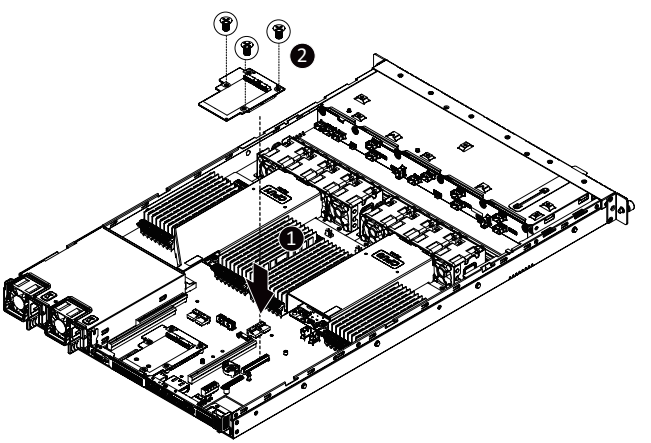
Follow these instructions to install a mezzanine card:

1. Insert the mezzanine card into the system ensuring that the connector on the mezzanine card connects to the connector on the motherboard.
2. Secure the mezzanine card to the system with three screws.

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R181-Z91/R181-Z92

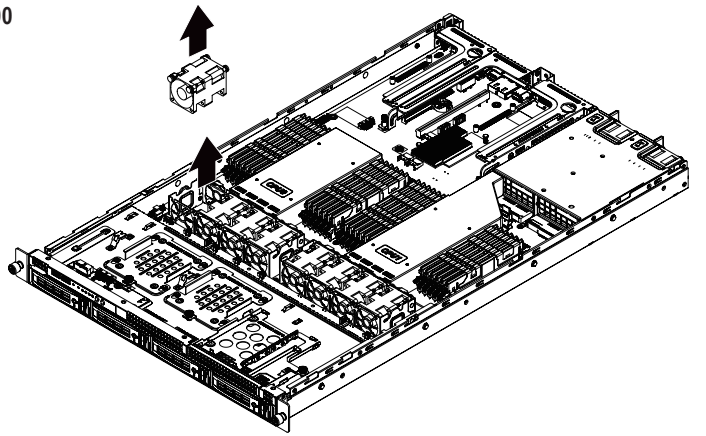


3-8 Replacing the FAN Assemblly

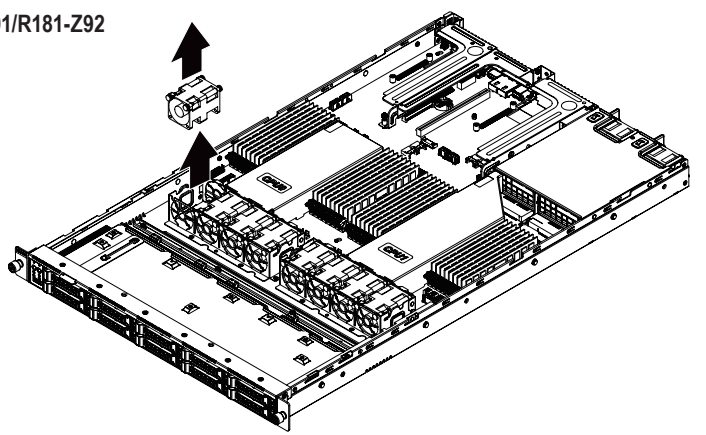
Follow these instructions to replace the fan assembly:

1. Lift up the fan assembly from the chassis.
2. Reverse the previous steps to install the replacement fan assembly.

R181-Z90



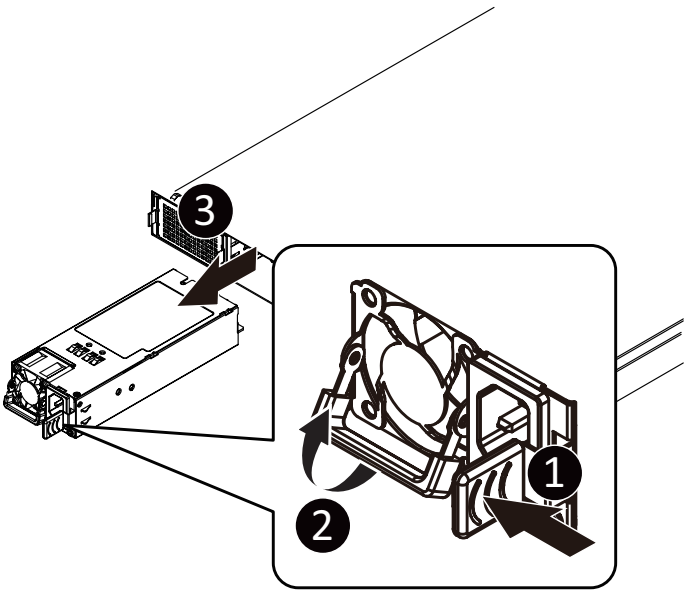
R181-Z91/R181-Z92



3-9 Replacing the Power Supply

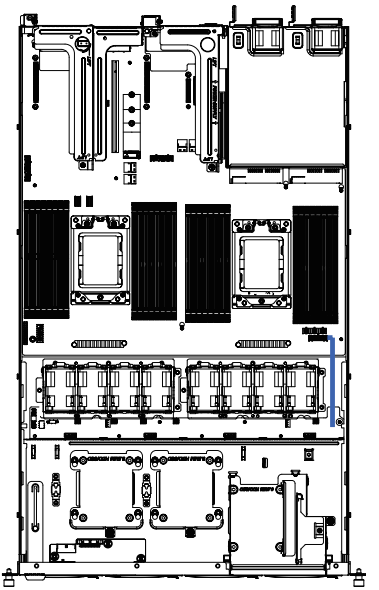
Follow these instructions to replace the power supply:

1. Press the retaining clip on the right side of the power supply along the direction of the arrow.
2. Pull up the power supply handle at the same time and pull out the power supply.
3. Insert the replacement power supply firmly into the chassis. Connect the AC power cord to the replacement power supply.

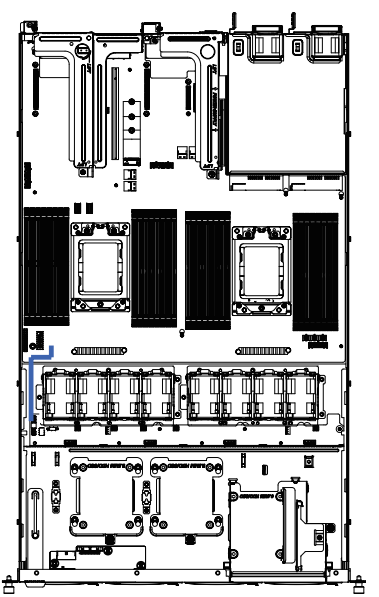


3-10 Cable Routing (R181-Z90)

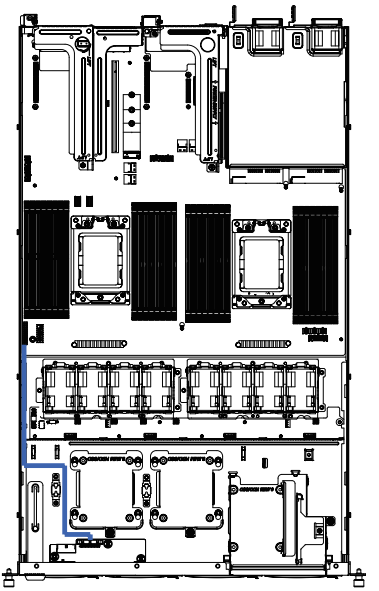
HDD Back Plane Board Power Cable



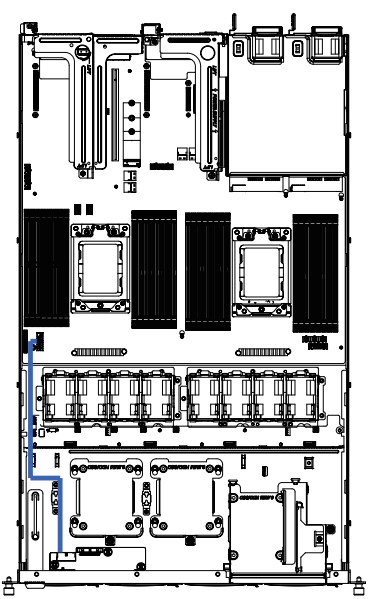
HDD Back Plane Board Signal Cable



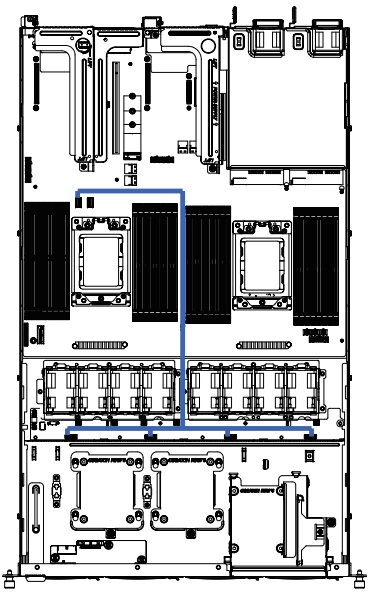
Front IO Board Cable



Front Panel USB 3.0 Cable

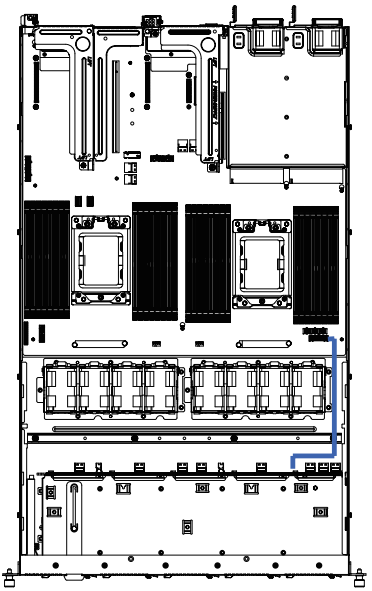


On-Board SATA to HDD Back Plane Board Cable

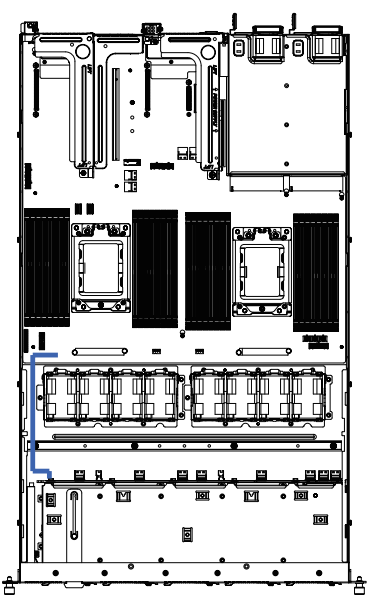


3-11 Cable Routing (R181-Z91/Z92)

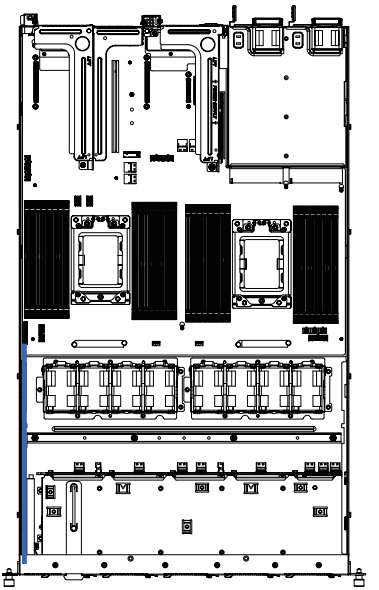
HDD Back Plane Board Power Cable



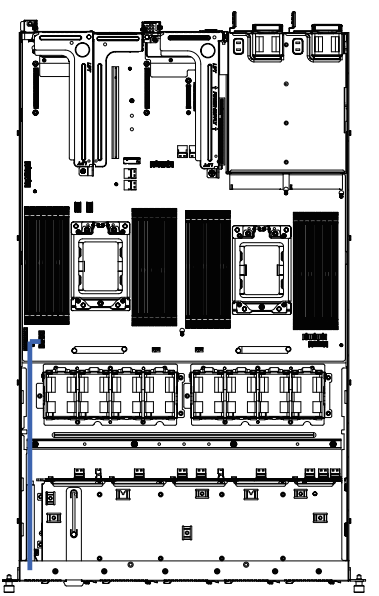
HDD Back Plane Board Signal Cable



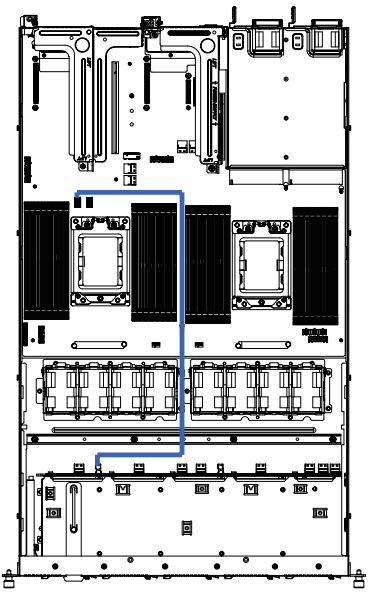
Front IO Board Cable



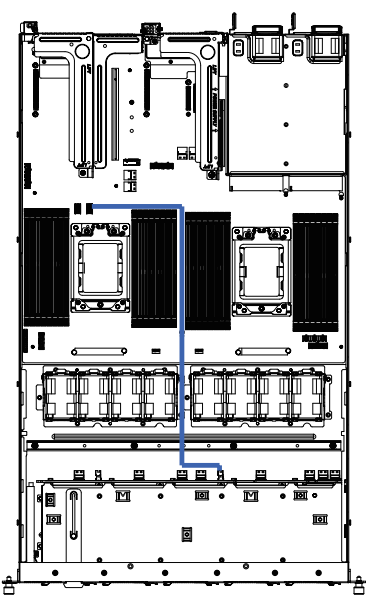
Front Panel USB 3.0 Cable



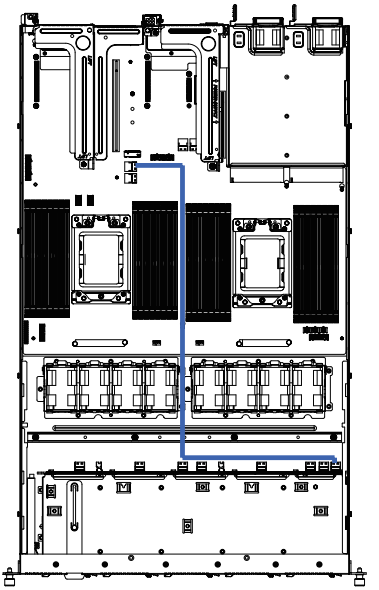
On-Board SATA to HDD Back Plane Board Cable (SATA0)



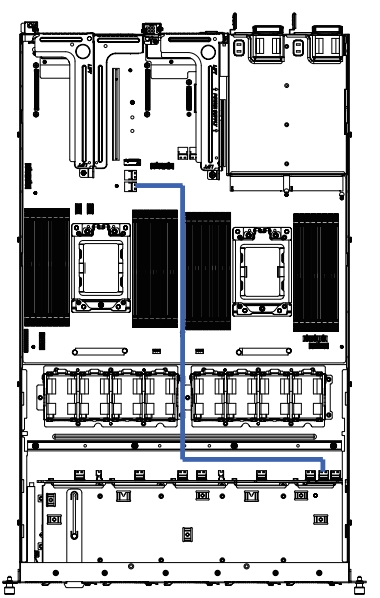
On-Board SATA to HDD Back Plane Board Cable (SATA1)



U.2 NMVe to HDD Back Plane Board Cable (NMVe0)

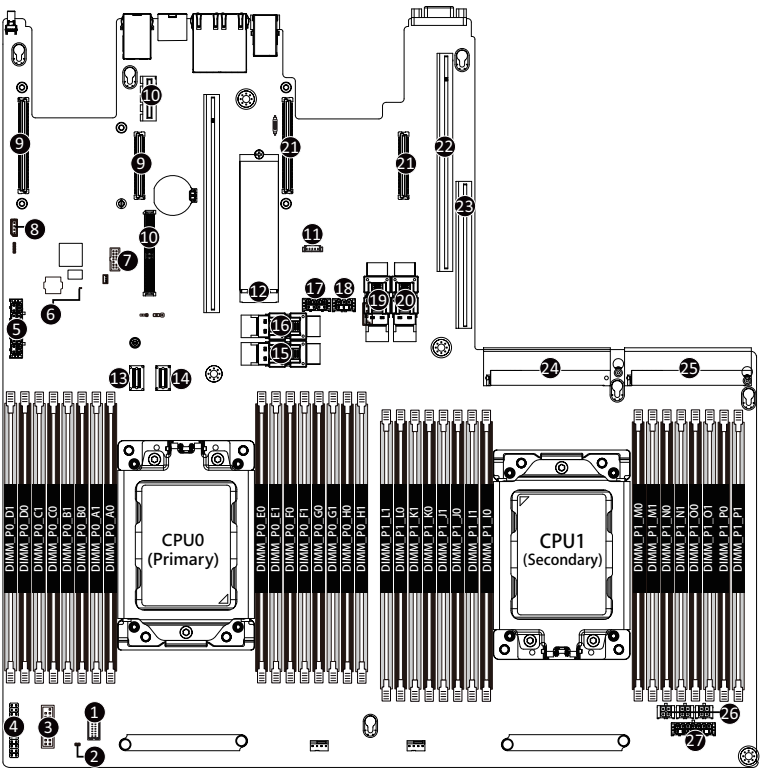


U.2 NMVe to HDD Back Plane Board Cable (NMVe1)



Chapter 4 Motherboard Components

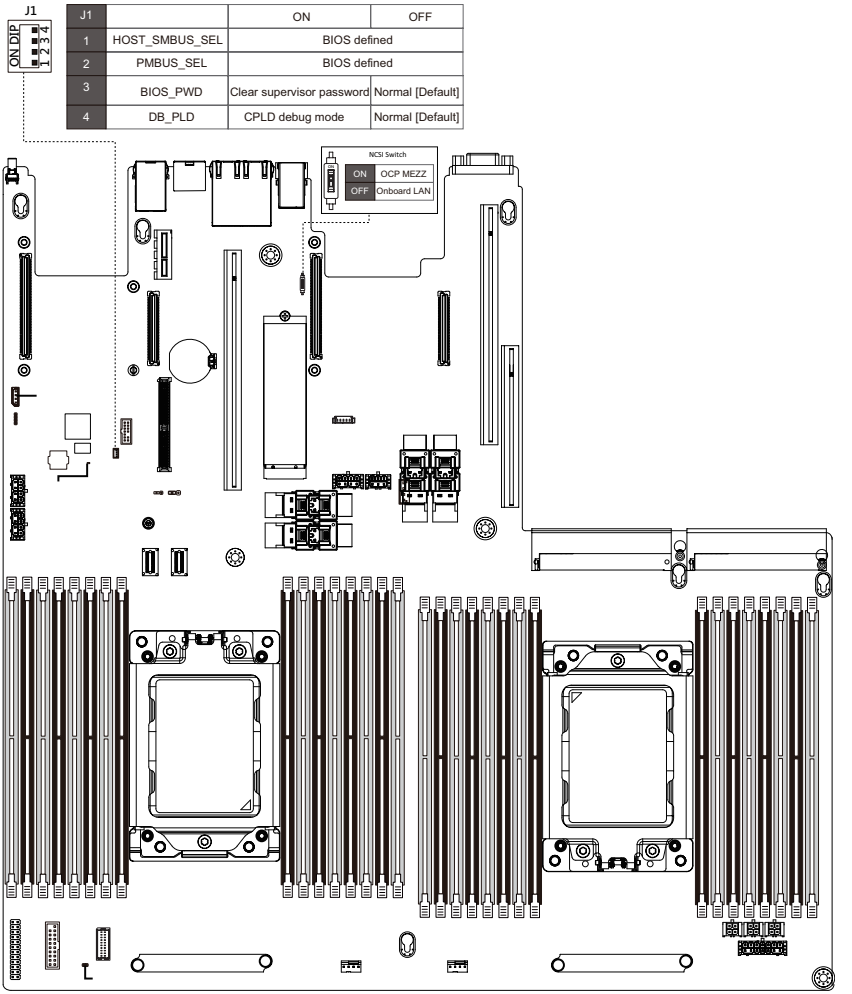
4-1 Motherboard Components



Item	Description
1	HDD Back Plane Board Connector
2	Case Open Intrusion Header
3	Front Panel USB 3.0 Connector
4	Front Panel Connector
5	2 x 4 Pi n GPGPU Power Connectors
6	BMC Firmware Readiness LED
7	TPM Modue Connector
8	IPMB Connector
9	OCP Mezzanine Connector#1 (Support NCSI)
10	Riser Slot Connector #1
11	SGPIO Connector
12	M.2 Slot (PCIe Gen3 x4, Support NGFF-2280, M-Key)
13	SlimLine Connector #0 (PCIe/SATA/Configurable and define SKUs)

14	SlimLine Connector #1 (PCIe/SATA/Configurable and define SKUs)
15	SlimLine Connector #3 (PCIe/SATA/Configurable and define SKUs)
16	SlimLine Connector #2 (PCIe/SATA/Configurable and define SKUs)
17	2 x 4 Pin GPGPU Power Connector
18	2 x 3 Pin Rear Back Plane Board Power Connector
19	SlimLine Connector #4 (PCIe/SATA/Configurable and define SKUs)
20	SlimLine Connector #5 (PCIe/SATA/Configurable and define SKUs)
21	OCP Mezzanine Connector#2
22	Riser Slot Connector #2
23	PCIe Slot Connector for Proprietary NVMe Small Card (R181-Z91/R181-Z92 Only)
24	Power Supply Connector#1 (Primary)
25	Power Supply Connector#2 (Secondary)
26	2 x 2 Pin Extention Card Power Connectors
27	2 x 7 Pin System Main Power Connector

4-2 Jumper Setting



J1		ON	OFF
1	HOST_SMBUS_SEL	BIOS defined	
2	PMBUS_SEL	BIOS defined	
3	BIOS_PWD	Clear supervisor password	Normal [Default]
4	DB_PLD	CPLD debug mode	Normal [Default]

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Chapter 5 BIOS Setup

BIOS (Basic Input and Output System) records hardware parameters of the system in the EFI on the motherboard. Its major functions include conducting the Power-On Self-Test (POST) during system startup, saving system parameters and loading operating system, etc. BIOS includes a BIOS Setup program that allows the user to modify basic system configuration settings or to activate certain system features. When the power is turned off, the battery on the motherboard supplies the necessary power to the CMOS to keep the configuration values in the CMOS.

To access the BIOS Setup program, press the <DEL> key during the POST when the power is turned on.



- BIOS flashing is potentially risky, if you do not encounter problems of using the current BIOS version, it is recommended that you don't flash the BIOS. To flash the BIOS, do it with caution. Inadequate BIOS flashing may result in system malfunction.
- It is recommended that you not alter the default settings (unless you need to) to prevent system instability or other unexpected results. Inadequately altering the settings may result in system's failure to boot. If this occurs, try to clear the CMOS values and reset the board to default values. (Refer to the **Exit** section in this chapter or introductions of the battery/clearing CMOS jumper in Chapter 4 for how to clear the CMOS values.)

BIOS Setup Program Function Keys

<←><→>	Move the selection bar to select the screen
<↑><↓>	Move the selection bar to select an item
<+>	Increase the numeric value or make changes
<->	Decrease the numeric value or make changes
<Enter>	Execute command or enter the submenu
<Esc>	Main Menu: Exit the BIOS Setup program Submenus: Exit current submenu
<F1>	Show descriptions of general help
<F3>	Restore the previous BIOS settings for the current submenus
<F9>	Load the Optimized BIOS default settings for the current submenus
<F10>	Save all the changes and exit the BIOS Setup program

- **Main**
  This setup page includes all the items in standard compatible BIOS.
- **Advanced**
  This setup page includes all the items of AMI BIOS special enhanced features.
  (ex: Auto detect fan and temperature status, automatically configure hard disk parameters.)
- **AMD CBS**
  This setup page includes the common items for configuration of AMD motherboard-related information.
- **AMD PBS Option**
  This setup page includes the common items for configuration of AMD CPM RAS related settings.
- **Chipset**
  This setup page includes all the submenu options for configuring the function of processor, network, North Bridge, South Bridge, and System event logs.
- **Server Management**
  Server additional features enabled/disabled setup menus.
- **Security**
  Change, set, or disable supervisor and user password. Configuration supervisor password allows you to restrict access to the system and BIOS Setup.
  A supervisor password allows you to make changes in BIOS Setup.
  A user password only allows you to view the BIOS settings but not to make changes.
- **Boot**
  This setup page provides items for configuration of boot sequence.
- **Save & Exit**
  Save all the changes made in the BIOS Setup program to the CMOS and exit BIOS Setup. (Pressing <F10> can also carry out this task.)
  Abandon all changes and the previous settings remain in effect. Pressing <Y> to the confirmation message will exit BIOS Setup. (Pressing <Esc> can also carry out this task.)

5-1 The Main Menu

Once you enter the BIOS Setup program, the Main Menu (as shown below) appears on the screen. Use arrow keys to move among the items and press <Enter> to accept or enter other sub-menu.

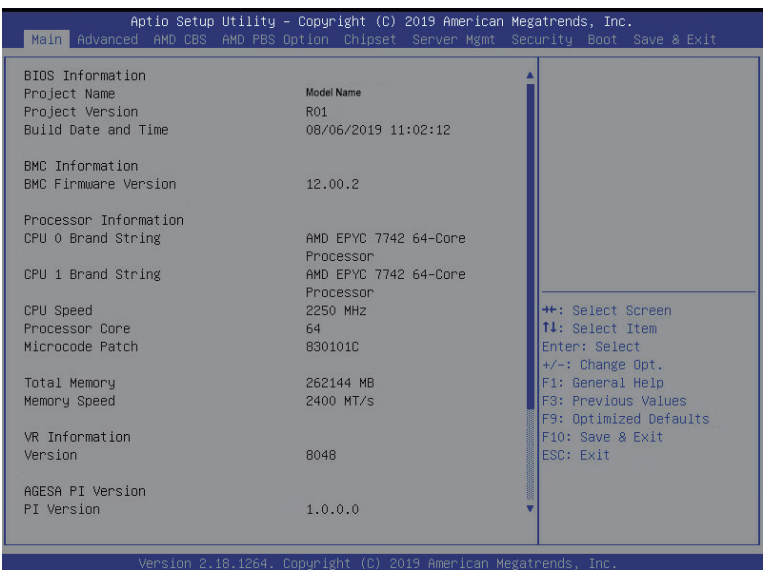
Main Menu Help

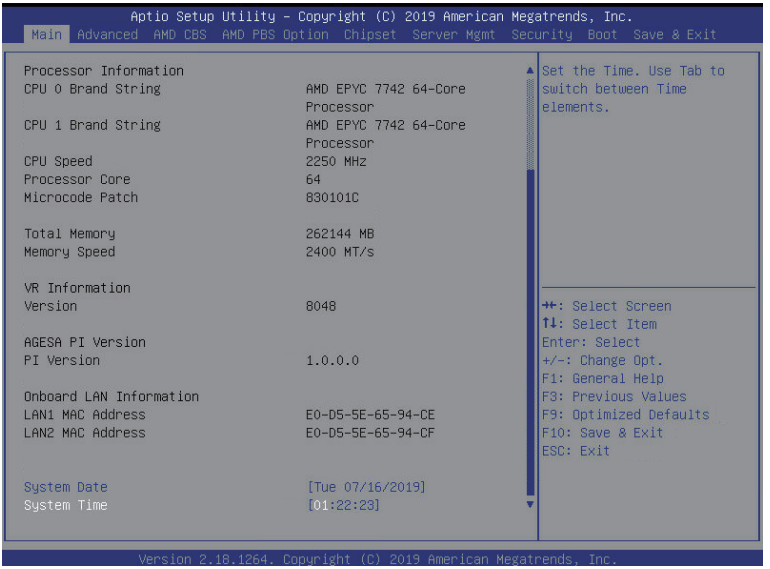
The on-screen description of a highlighted setup option is displayed on the bottom line of the Main Menu.

Submenu Help

While in a submenu, press <F1> to display a help screen (General Help) of function keys available for the menu. Press <Esc> to exit the help screen. Help for each item is in the Item Help block on the right side of the submenu.

- When the system is not stable as usual, select the **Restore Defaults** item to set your system to its defaults.
- The BIOS Setup menus described in this chapter are for reference only and may differ by BIOS version.





Parameter	Description
BIOS Information	
Project Name	Displays the project name information.
Project Version	Displays version number of the BIOS setup utility.
Build Date and Time	Displays the date and time when the BIOS setup utility was created.
BMC Information	
BMC Firmware Version	Displays version number of the BIOS setup utility.
BIOS Information	
Project Name	Displays the project name information.
Project Version	Displays version number of the BIOS setup utility.
Build Date and Time	Displays the date and time when the BIOS setup utility was created.
BMC Information	
BMC Firmware Version	Displays version number of the BIOS setup utility.
Processor Information	
CPU 0 Brand String / CPU 1 Brand String / CPU Speed / Processor Core / Microcode Patch	Displays the technical information for the installed processor(s).

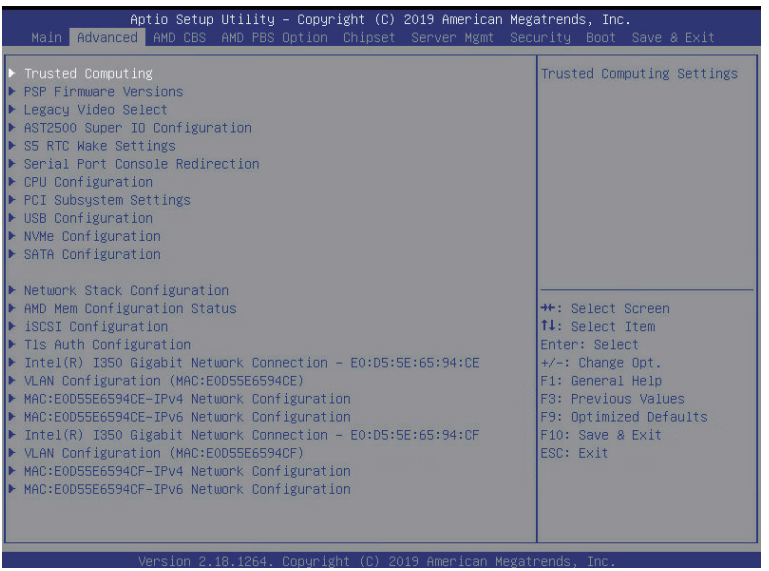
Parameter	Description
Total Memory(Note1)	Displays the total memory size of the installed memory.
Memory Speed(Note1)	Displays the frequency information of the installed memory.
VR Information	
Version	Displays VR version information.
AGESA PI Version	
PI Version	Displays AGESA PI version information.
Onboard LAN Information	
LAN1 MAC Address(Note2)	Displays LAN MAC address information.
LAN2 MAC Address(Note2)	Displays LAN MAC address information.
System Date	Sets the date following the weekday-month-day-year format.
System Time	Sets the system time following the hour-minute-second format.

(Note1) The number of LAN ports listed will depend on the motherboard / system model.

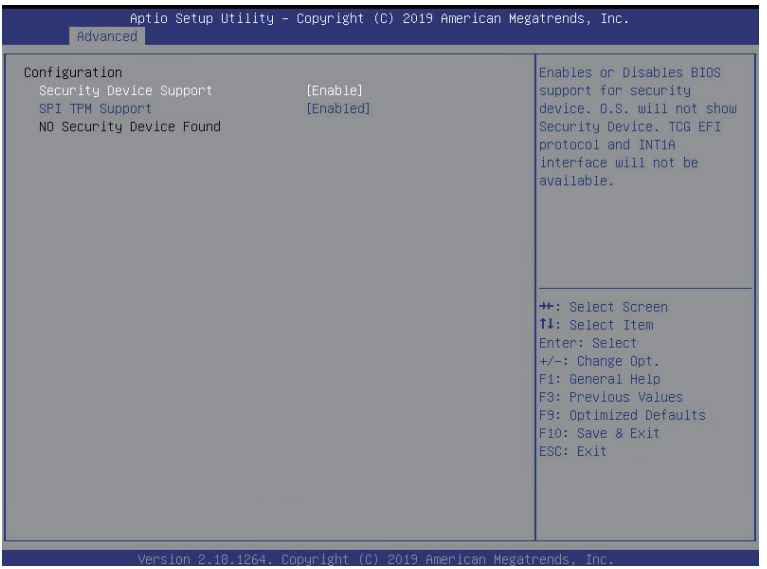
(Note2) This section will display capacity and frequency information of the memory that the customer has installed.

5-2 Advanced Menu

The Advanced menu display submenu options for configuring the function of various hardware components. Select a submenu item, then press [Enter] to access the related submenu screen.



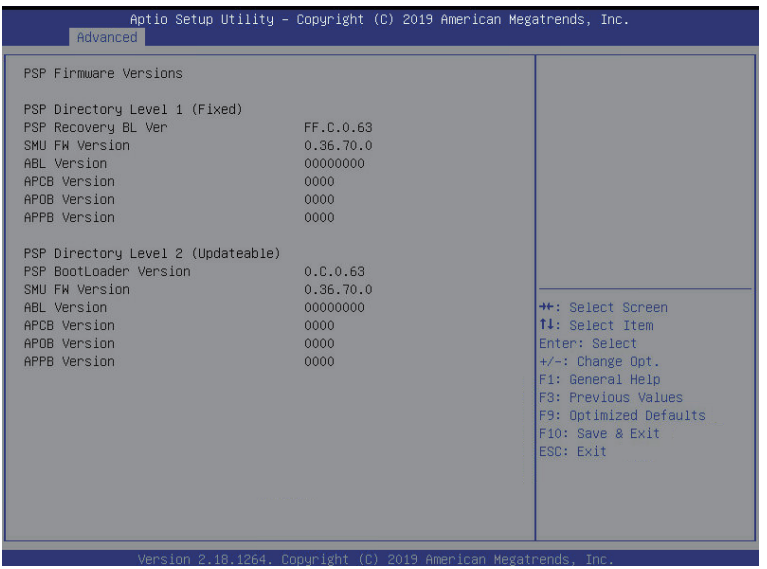
5-2-1 Trusted Computing



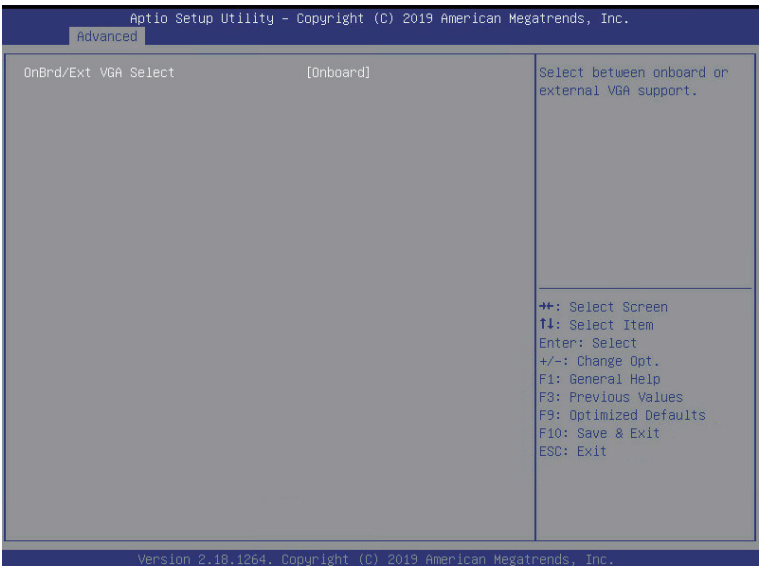
Parameter	Description
Configuration	
Security Device Support	Select Enable to activate TPM support feature. Options available: Enable/Disable. Default setting is **Enable**.
SPI TPM Support	Options available: Enabled/Disabled. Default setting is **Enabled**

5-2-2 PSP Firmware Versions

The PSP Firmware Versions page displays the basic PSP firmware version information. Items on this window are non-configurable.

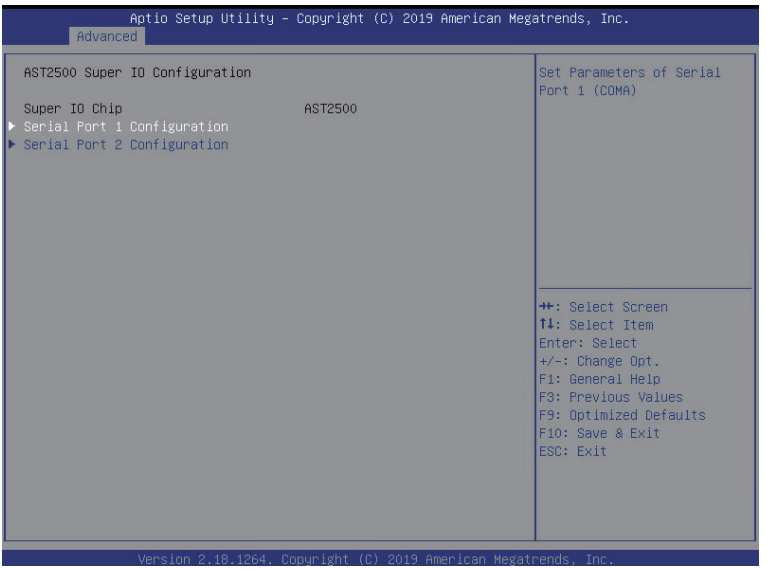


5-2-3 Legacy Video Select



Parameter	Description
OnBrd/Ext VGA Select	Select between onboard or external VGA support. Options available: Auto/Onboard/External. Default setting is **Onboard**.

5-2-4 AST2500 Super IO Configuration



Parameter	Description
AST2500 Super IO Configuration	
Super IO Chip	Displays the super IO chip information.

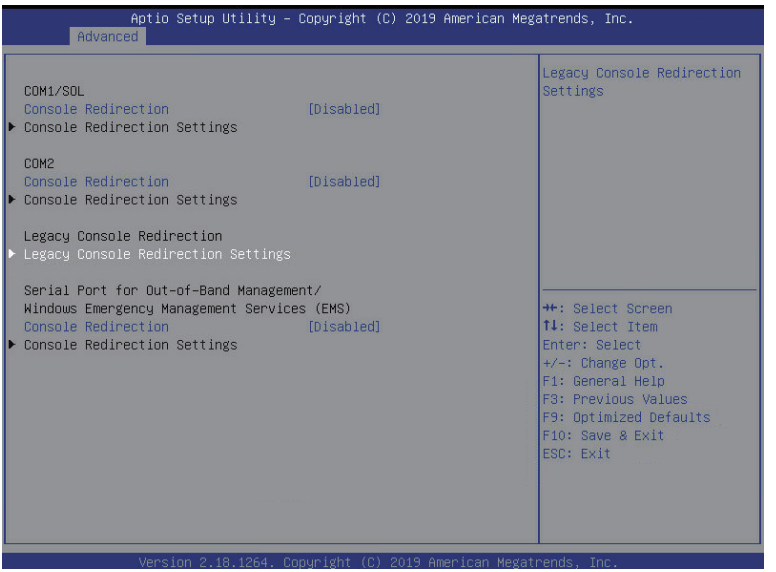
Parameter	Description
Serial Port 1/2 Configuration	Press [Enter] to configure advanced items. ◆ Serial Port(Note1): – Enable/Disable the Serial Port (COM). When set to Enabled allows you to configure the Serial port 1/2 settings. When set to Disabled, displays no configuration for the serial port. – Options available: Enabled/Disabled. Default setting is **Enabled**. ◆ Devices Settings(Note2): – Displays the serial port 1/2 device settings. ◆ Change Settings(Note2): – Select an optimal setting for the Super I/O device: – Options available for Serial Port 1: Auto IO=3F8h; IRQ=4; IO=3F8h; IRQ=3, 4, 5, 6, 7, 9, 10, 11, 12; IO=2F8h; IRQ=3, 4, 5, 6, 7, 9, 10, 11, 12; IO=3E8h; IRQ=3, 4, 5, 6, 7, 9, 10, 11, 12; IO=2E8h; IRQ=3, 4, 5, 6, 7, 9, 10, 11, 12; Default setting is **Auto**. Options available for Serial Port 2: Auto IO=2F8h; IRQ=3; IO=3F8h; IRQ=3, 4, 5, 6, 7, 9, 10, 11, 12; IO=2F8h; IRQ=3, 4, 5, 6, 7, 9, 10, 11, 12; IO=3E8h; IRQ=3, 4, 5, 6, 7, 9, 10, 11, 12; IO=2E8h; IRQ=3, 4, 5, 6, 7, 9, 10, 11, 12; Default setting is **Auto**. (Note1) Advanced items will appear when this item is set to **Enabled**. (Note2) This item will appear when **Serial Port** is set to **Enabled**.

5-2-5 S5 RTC Wake Settings



Parameter	Description
Wake system from S5	Enable or disable system wake on alarm event. Select Fixed Time, system will wake on the time (HH:MM:SS) specified. Select Dynamic Time and the system will wake at the current time plus an increase in minute(s). Options available: Disabled/Fixed Time. Default setting is **Disabled**.

5-2-6 Serial Port Console Redirection



Parameter	Description
COM1/SOL / COM2 Console Redirection(Note)	Select whether to enable console redirection for specified device. Console redirection enables the users to manage the system from a remote location. Options available: Enabled/Disabled. Default setting is **Disabled**.
Legacy Console Redirection	Selects a COM port for Legacy serial redirection. The options are dependent on the available COM ports.
Serial Port for Out-of-Band Management / Windows Emergency Management Services (EMS) Console Redirection(Note)	Selects a COM port for EMS console redirection. EMS console redirection allows the user to configure Console Redirection Settings to support Out-of-Band Serial Port management. Options available: Enabled/Disabled. Default setting is **Disabled**.
COM1/SOL / COM2 Console Redirection Settings	Press [Enter] to configure advanced items. **Please note that this item is configurable when COM1/SOL / COM2 Console Redirection is set to Enabled.** ◆ Terminal Type – Selects a terminal type to be used for console redirection. – Options available: VT100/VT100+/ANSI /VT-UTF8. Default setting is **ANSI**.

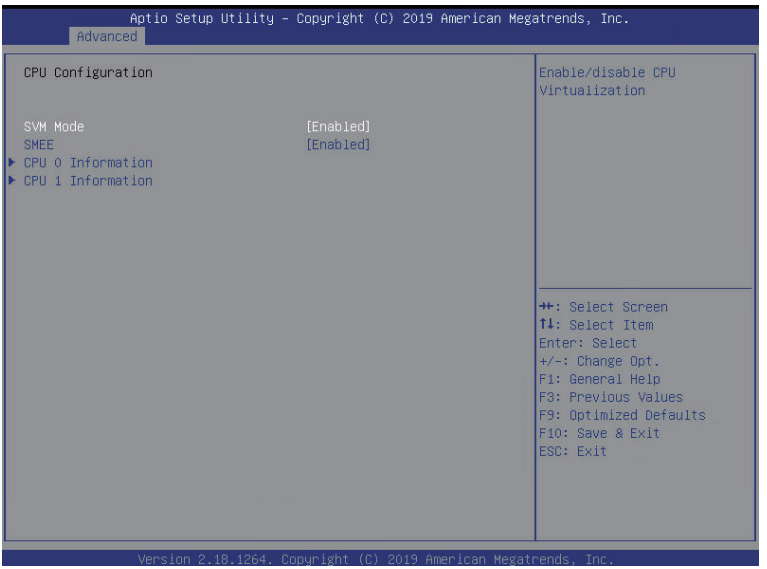
(Note) Advanced items prompt when this item is set to Enabled.

Parameter	Description
COM1/SOL / COM2 Console Redirection Settings (continued)	◆ Bits per second – Selects the transfer rate for console redirection. – Options available: 9600/19200/38400/57600/115200. Default setting is **115200**. ◆ Data Bits – Selects the number of data bits used for console redirection. – Options available: 7/8. Default setting is **8**. ◆ Parity – A parity bit can be sent with the data bits to detect some transmission errors. – Even: parity bit is 0 if the num of 1's in the data bits is even. – Odd: parity bit is 0 if num of 1's in the data bits is odd. – Mark: parity bit is always 1. Space: Parity bit is always 0. – Mark and Space Parity do not allow for error detection. – Options available: None/Even/Odd/Mark/Space. Default setting is **None**. ◆ Stop Bits – Stop bits indicate the end of a serial data packet. (A start bit indicates the beginning). The standard setting is 1 stop bit. Communication with slow devices may require more than 1 stop bit. – Options available: 1/2. Default setting is **1**. ◆ Flow Control – Flow control can prevent data loss from buffer overflow. When sending data, if the receiving buffers are full, a 'stop' signal can be sent to stop the data flow. Once the buffers are empty, a 'start' signal can be sent to re-start the flow. Hardware flow control uses two wires to send start/stop signals. – Options available: None/Hardware RTS/CTS. Default setting is **None**. ◆ VT-UTF8 Combo Key Support – Enable/Disable the VT-UTF8 Combo Key Support. – Options available: Enabled/Disabled. Default setting is **Enabled**. ◆ Recorder Mode(Note) – When this mode enabled, only texts will be send. This is to capture Terminal data. – Options available: Enabled/Disabled. Default setting is **Disabled**. ◆ Resolution 100x31(Note) – Enable/Disable extended terminal resolution. – Options available: Enabled/Disabled. Default setting is **Enabled**. ◆ Putty KeyPad(Note) – Selects FunctionKey and KeyPad on Putty. – Options available: T100/LINUX/XTERMR6/SCO/ESCN/VT400. – Default setting is VT100.

(Note) Advanced items prompt when this item is defined.

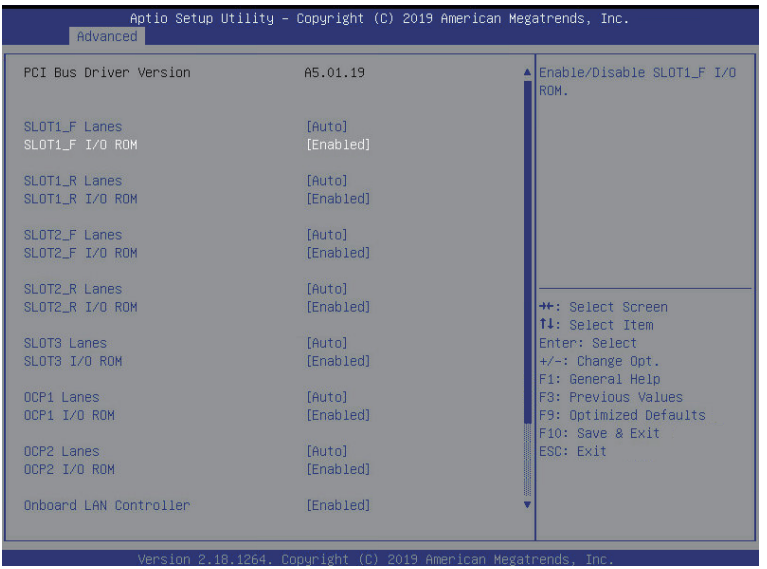
Parameter	Description
Legacy Console Redirection Settings	◆ Redirection COM Port – Selects a COM port to display redirection of Legacy OS and Legacy OPROM Messages. – Options available: COM1/SOL / COM2. Default setting is **COM1/ SOL**. ◆ Resolution – On Legacy OS, the number of rows and columns supported in redirection. ◆ Options available: 80x24/80x25. Default setting is **80x24**. ◆ Redirection After BIOS POST – This item allows user to enable console redirection after OS has loaded. – Options available: Always Enable/Boot Loader. Default setting is **Always Enable**.
Serial Port for Out-of-Band Management / Windows Emergency Management Services (EMS) Console Redirection Settings	◆ Out-of-Band Mgmt Port – Selects a serial port to remotely manage a Windows server OS. – Options available: COM1/SOL / COM2. Default setting is **COM1/ SOL**. ◆ Terminal Type – Selects a terminal type to be used for console redirection. – Options available: VT100/VT100+/ANSI /VT-UTF8. Default setting is **VT-UTF8**. ◆ Bits per second – Selects the transfer rate for console redirection. – Options available: 9600/19200/38400/57600/115200. Default setting is **115200**. ◆ Flow Control – Flow control can prevent data loss from buffer overflow. When sending data, if the receiving buffers are full, a 'stop' signal can be sent to stop the data flow. Once the buffers are empty, a 'start' signal can be sent to re-start the flow. Hardware flow control uses two wires to send start/stop signals. – Options available: None/Hardware RTS/CTS. Default setting is **None**.

5-2-7 CPU Configuration



Parameter	Description
CPU Configuration	
SVM Mode	Enable/disable the CPU Virtualization. Options available: Enabled/Disabled. Default setting is **Enabled**.
SMEE	Controls the Secure Memory Encryption Enable (SMEE) function. Options available: Enabled/Disabled. Default setting is **Enabled**.
CPU 0 Information	Press [Enter] to view more information related to CPU 0.
CPU 1 Information	Press [Enter] to view more information related to CPU 1.

5-2-8 PCI Subsystem Settings



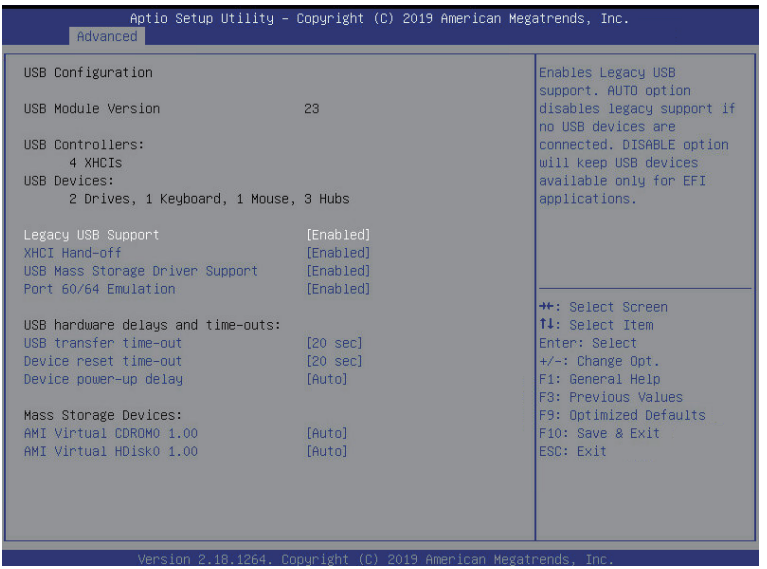
Parameter	Description
PCI Bus Driver Version	Displays the PCI Bus Driver version information.
SLOT1_F / SLOT1_R / SLOT2_F / SLOT2_R / SLOT3 / OCP1 / OCP2 Lanes(Note1)	Change the PCIe lanes. Options available: Auto / x16 / x8 x8 / x8 x4 x4 / x4 x4 x8 / x4 x4 x4 x4 (OCP2 Lanes only features Auto / x8 / x4 x4.) Disabled. Default setting is **Auto**.
SLOT1_F / SLOT1_R / SLOT2_F / SLOT2_R / SLOT3 / OCP1 / OCP2 I/O ROM(Note1)	When enabled, this setting will initialize the device expansion ROM for the related PCI-E slot. Options available: Enabled/Disabled. Default setting is **Enabled**.
Onboard LAN Controller(Note2)	Enable/Disable the onboard LAN devices. Options available: Enabled/Disabled. Default setting is **Enabled**.
Onboard LAN I/O ROM(Note2)	Enable/Disable the onboard LAN devices and initializes device expansion ROM. Options available: Enabled/Disabled. Default setting is **Enabled**.
PCI Devices Common Settings	
Above 4G Decoding	Enable/Disable memory mapped I/O to 4GB or greater address space (Above 4G Decoding). Options available: Enabled/Disabled. Default setting is **Enabled**.

(Note1) This section is dependent on the available PCIe Slot.

(Note2) This section is dependent on the available LAN controller.

Parameter	Description
SR-IOV Support	If the system has SR-IOV capable PCIe devices, this item Enable/Disable Single Root IO Virtualization Support. Options available: Enabled/Disabled. Default setting is **Enabled**.

5-2-9 USB Configuration

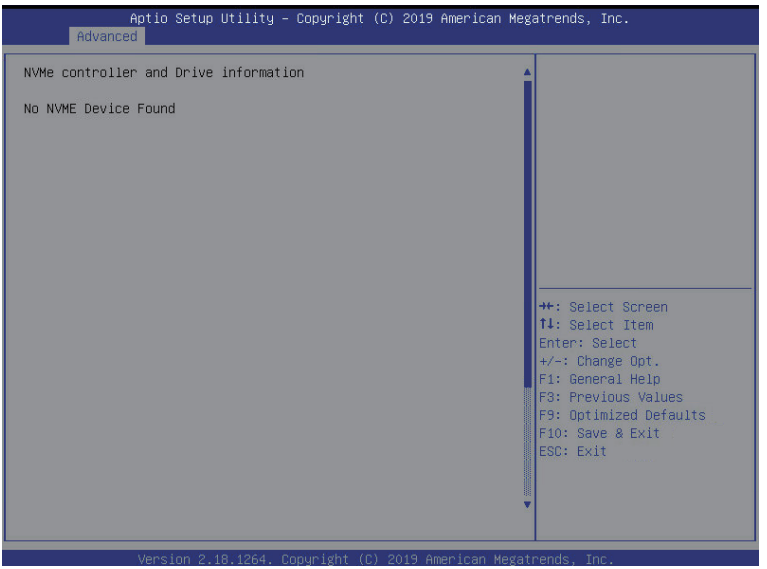


Parameter	Description
USB Configuration	
USB Module Version	Displays the USB version.
USB Controllers	Displays the supported USB controllers.
USB Devices	Displays the USB devices connected to the system.
Legacy USB Support	Enable/disable the Legacy USB support fuction. AUTO option disables legacy support if no USB devices are connected. DISABLE option will keep USB devices available only for EFI applications. Options available: Auto/Enabled/Disabled. Default setting is **Enabled**.
XHCI Hand-off	Enable/Disable the XHCI (USB 3.0) Hand-off support. Options available: Enabled/Disabled. Default setting is **Enabled**.
USB Mass Storage Driver Support(Note)	Enable/Disable the USB Mass Storage Driver Support. Options available: Enabled/Disabled. Default setting is **Enabled**.
Port 60/64 Emulation	Enables the I/O port 60h/64h emulation support. This should be enabled for the complete USB Keyboard Legacy support for non-USB aware OS. Options available: Enabled/Disabled. Default setting is **Enabled**.
USB hardware delays and time-outs	
USB transfer time out	The time-out value for Control, Bulk, and Interrupt transfers. Options available: 1 sec/5 sec/10 sec/20 sec. Default setting is **20 sec**.

(Note) This item is present only if you attach USB devices.

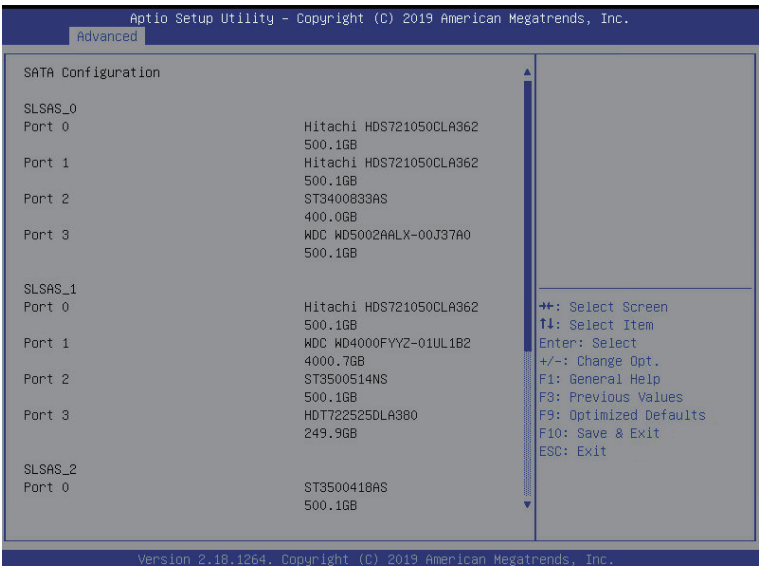
Parameter	Description
Device reset time-out	USB mass storage device Start Unit command time-out. Options available: 10 sec/20 sec/30 sec/40 sec. Default setting is **20 sec**.
Device power-up delay	Maximum time the device will take before it properly reports itself to the Host Controller. "Auto" uses default value: for a Root port it is 100 ms, for a Hub port the delay is taken from Hub descriptor. Options available: Auto/Manual. Default setting is **Auto**.
Mass Storage Devices	
AMI Virtual CDROM0 1.00 / HDisk0 1.00	Mass storage device emulation type. AUTO enumerates devices according to their media format. Optical drives are emulated as CDROM, drives with no media will be emulated according to a drive type. Options available: Auto/Floppy/Forced FDD/Hard Disk/CD-ROM. Default setting is **Auto**.

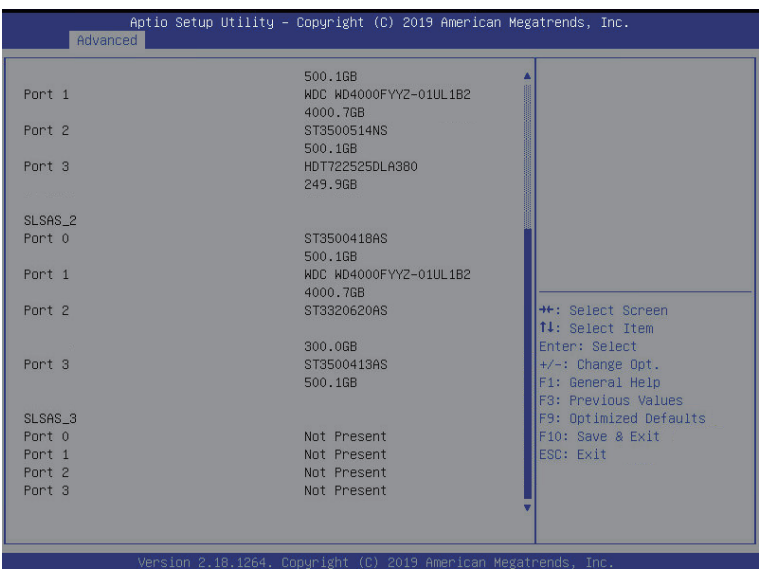
5-2-10 NVMe Configuration



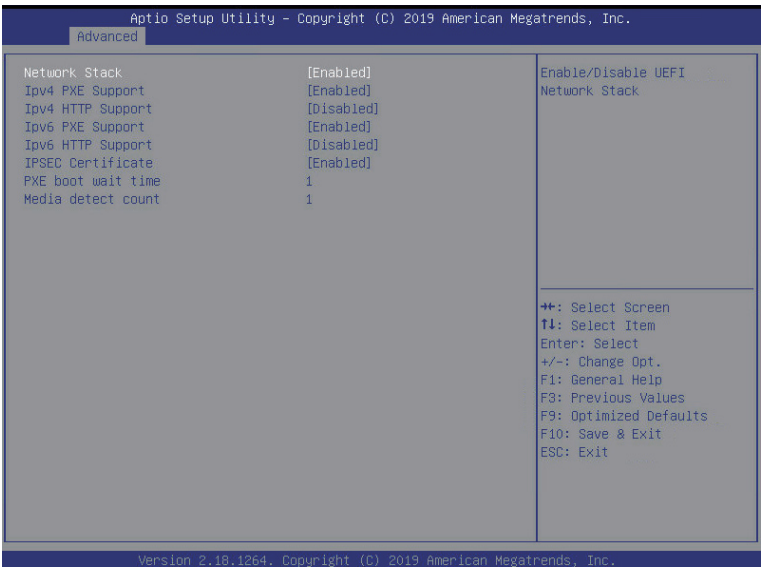
Parameter	Description
NVMe controller and Drive Information	Displays the NVMe devices connected to the system.

5-2-11 SATA Configuration





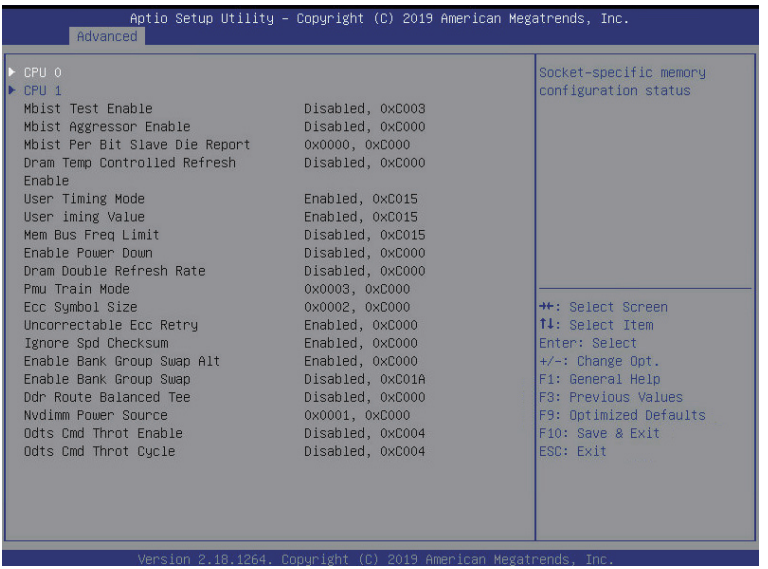
5-2-12 Network Stack Configuration



Parameter	Description
Network Stack	Enable/Disable the UEFI network stack. Options available: Enabled/Disabled. Default setting is **Enabled**.
Ipv4 PXE Support(Note)	Enable/Disable the Ipv4 PXE feature. Options available: Enabled/Disabled. Default setting is **Enabled**.
Ipv4 HTTP Support(Note)	Enable/Disable the Ipv4 HTTP feature. Options available: Enabled/Disabled. Default setting is **Disabled**.
Ipv6 PXE Support(Note)	Enable/Disable the Ipv6 PXE feature. Options available: Enabled/Disabled. Default setting is **Disabled**.
Ipv6 HTTP Support(Note)	Enable/Disable the Ipv6 HTTP feature. Options available: Enabled/Disabled. Default setting is **Disabled**.
IPSEC Certificate(Note)	Enable/Disable the IPSEC Certificate feature.
PXE boot wait time(Note)	Wait time in seconds to press ESC key to abort the PXE boot. Press the <+> / <-> keys to increase or decrease the desired values.
Media detect count(Note)	Number of times the presence of media will be checked. Press the <+> / <-> keys to increase or decrease the desired values.

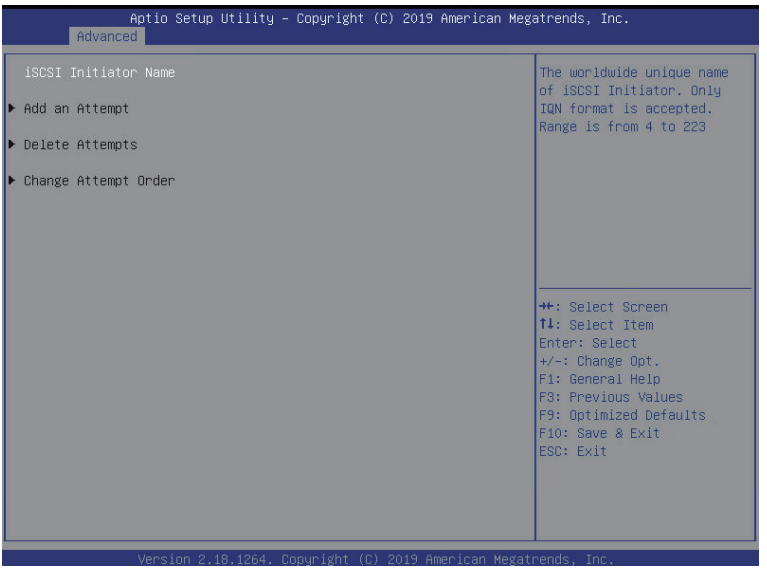
(Note) This item appears when **Network Stack** is set to **Enabled**.

5-2-13 AMD Mem Configuration Status



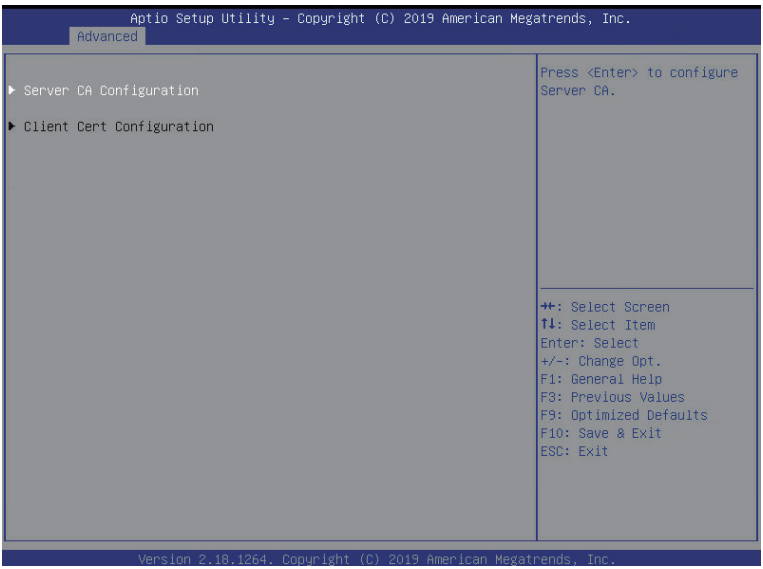
Parameter	Description
CPU 0	Press [Enter] for configuration of advanced items. ◆ Channel A/BC/D/E/F/G/H – DIMM0 Presence – DIMM1 Presence – Chipset/Bank Interleave ◆ Dram EC ◆ Dram Parity ◆ Dimm Sensor Fine Grain Mode
CPU 1	Press [Enter] for configuration of advanced items. ◆ Channel I/J/K/L/M/N/O/P – DIMM0 Presence – DIMM1 Presence – Chipset/Bank Interleave ◆ Dram EC ◆ Dram Parity ◆ Dimm Sensor Fine Grain Mode

5-2-14 iSCSI Configuration



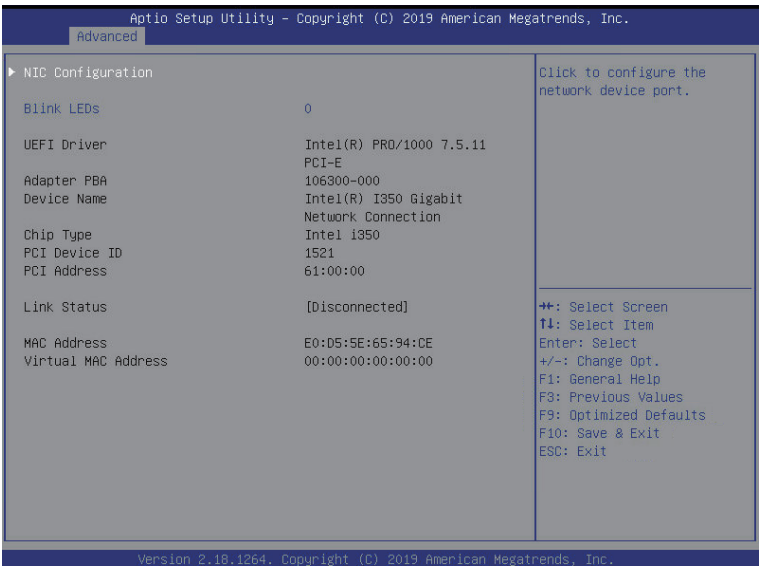
Parameter	Description
iSCSI Initiator Name	Press [Enter] and name iSCSI Initiator. Only IQN format is accecpted. Range: from 4 to 223
Add Attempt	Press [Enter] for configuration of advanced items.
Delete Attempt	Press [Enter] for configuration of advanced items.
Change Attempt Order	Press [Enter] for configuration of advanced items.

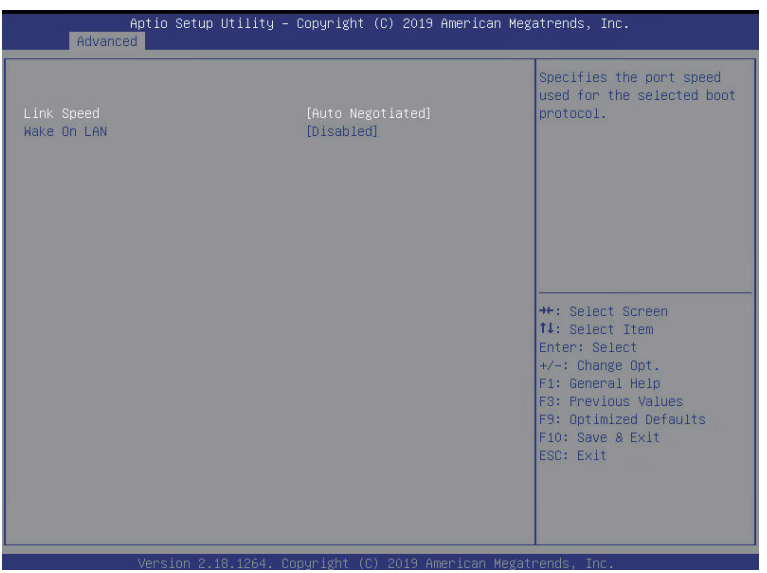
5-2-15 Tls Auth Configuration



Parameter	Description
Server CA Configuration	Press [Enter] for configuration of advanced items. ◆ Enroll Cert – Press [Enter] to enroll a certificate • Enroll Cert Using File • Cert GUID Input digit character in 1111111-2222-3333-4444-1234567890ab format. – Commit Changes and Exit – Discard Changes and Exit ◆ Delete Cert
Client Cert Configuration	N/A

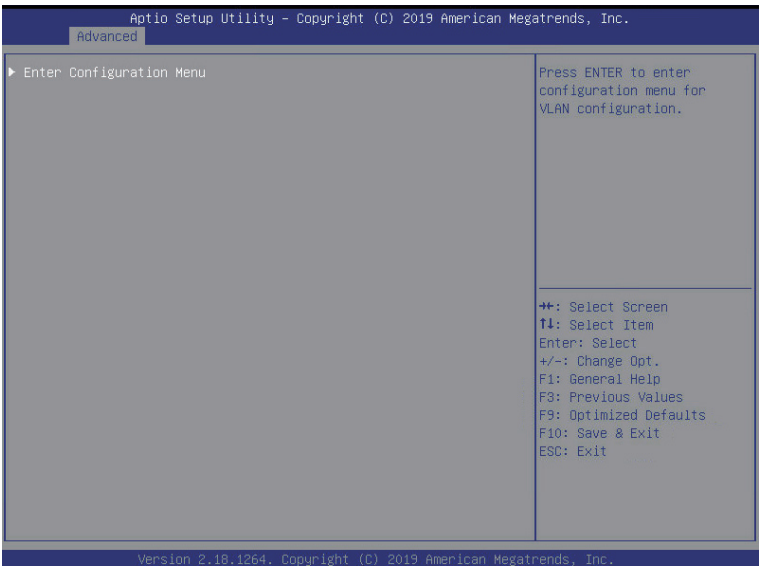
5-2-16 Intel(R) I350 Gigabit Network Connection

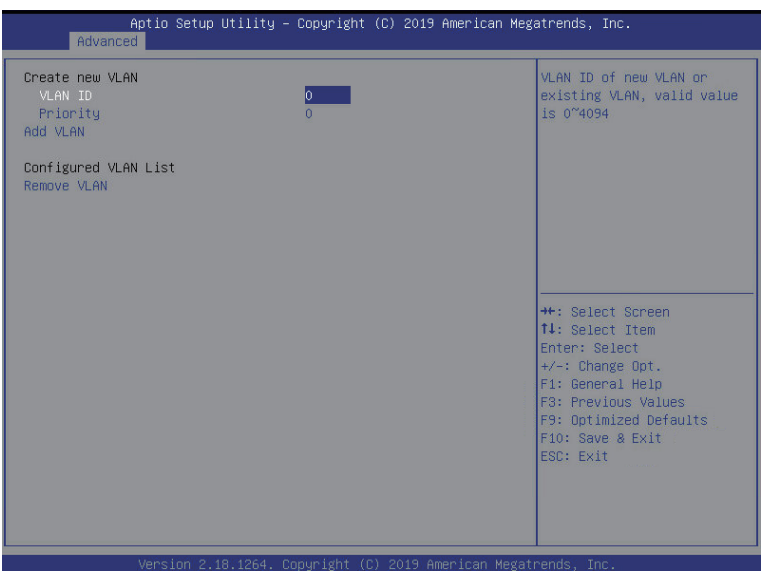




Parameter	Description
NIC Configuration	Press [Enter] to configure advanced items. ◆ Link Speed – Allows for automatic link speed adjustment. – Options available: Auto Negotiated/10 Mbps Half/10 Mbps Full/100 Mbps Half/100 Mbps Full. Default setting is **Auto Negotiated**. ◆ Wake On LAN – Enables power on of the system via LAN. Note that configuring Wake on LAN in the operating system does not change the value of this setting, but does override the behavior of Wake on LAN in OS controlled power states. – Options available: Enabled/Disabled. Default setting is **Enabled**.
Blink LEDs	Identifies the physical network port by blinking the associated LED. Press the numeric keys to adjust desired values.
UEFI Driver	Displays the technical specifications for the Network Interface Controller.
Adapter PBA	Displays the technical specifications for the Network Interface Controller.
Device Name	Displays the technical specifications for the Network Interface Controller.
Chip Type	Displays the technical specifications for the Network Interface Controller.
PCI Device ID	Displays the technical specifications for the Network Interface Controller.
PCI Address	Displays the technical specifications for the Network Interface Controller.
Link Status	Displays the technical specifications for the Network Interface Controller.
MAC Address	Displays the technical specifications for the Network Interface Controller.
Virtual MAC Address	Displays the technical specifications for the Network Interface Controller.

5-2-17 VLAN Configuration

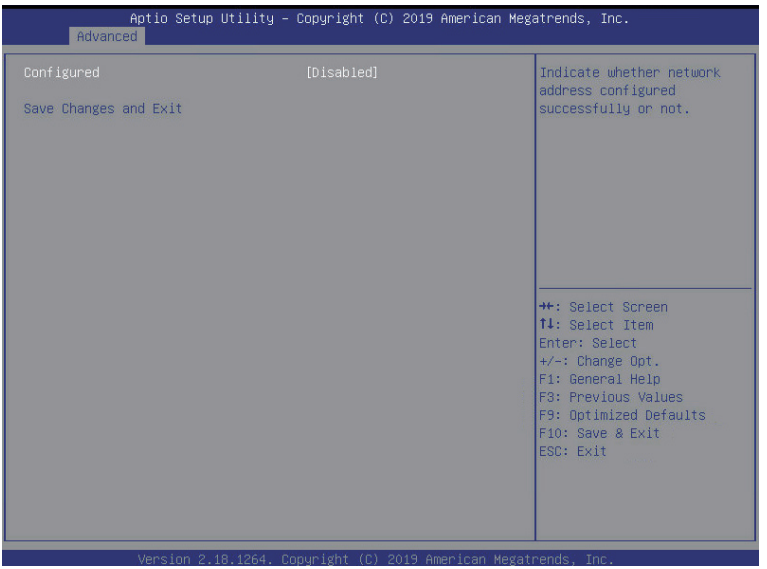




Parameter	Description
Enter Configuration Menu	Press [Enter] to configure advanced items. ◆ Create new VLAN ◆ VLAN ID – Sets VLAN ID for a new VLAN or an existing VLAN. – Press the <+> / <-> keys to increase or decrease the desired values. The valid range is from 0 to 4094. ◆ Priority – Sets 802.1Q Priority for a new VLAN or an existing VLAN. – Press the <+> / <-> keys to increase or decrease the desired values. The valid range is from 0 to 7. ◆ Add VLAN – Press [Enter] to create a new VLAN or update an existing VLAN. ◆ Configured VLAN List – Enable/Disable the VLAN. – Options available: Enable/Disable. Default setting is **Disabled**. ◆ Remove VLAN – Press [Enter] to remove an existing VLAN.

(Note) Only Supported when **Configured VLAN List** is set to **Enabled**.

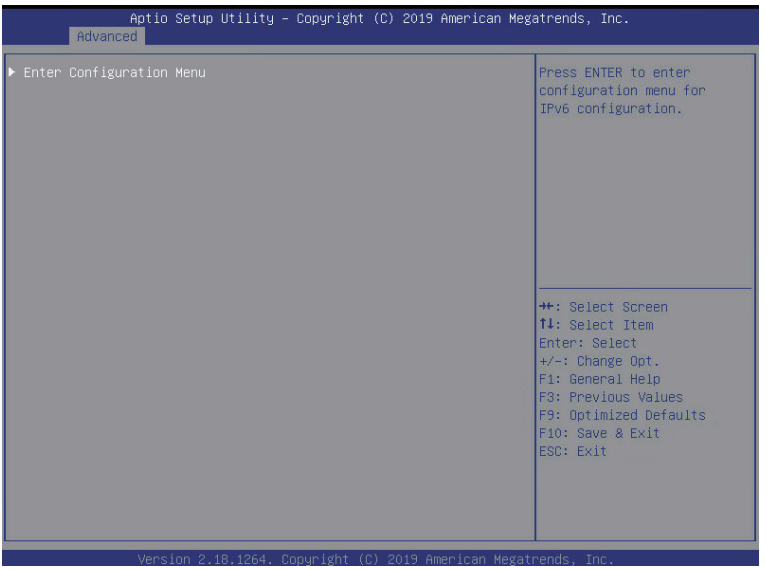
5-2-18 MAC IPv4 Network Configuration



Parameter	Description
Configured	Indicates whether network address is configured successfully or not. Options available: Disabled/Enabled. Default setting is **Disabled**.
Enable DHCP(Note)	Options available: Enabled/Disabled. Default setting is **Enabled**.
Local IP Address(Note)	Press [Enter] to configure local IP address.
Local NetMask(Note)	Press [Enter] to configure local NetMask.
Local Gateway(Note)	Press [Enter] to configure local Gateway
Local DNS Servers(Note)	Press [Enter] to configure local DNS servers
Save Changes and Exit	Press [Enter] and then choose to save or discard the changes made.

(Note) This item will appear on the screen when **Configured** is set to **Enabled**.

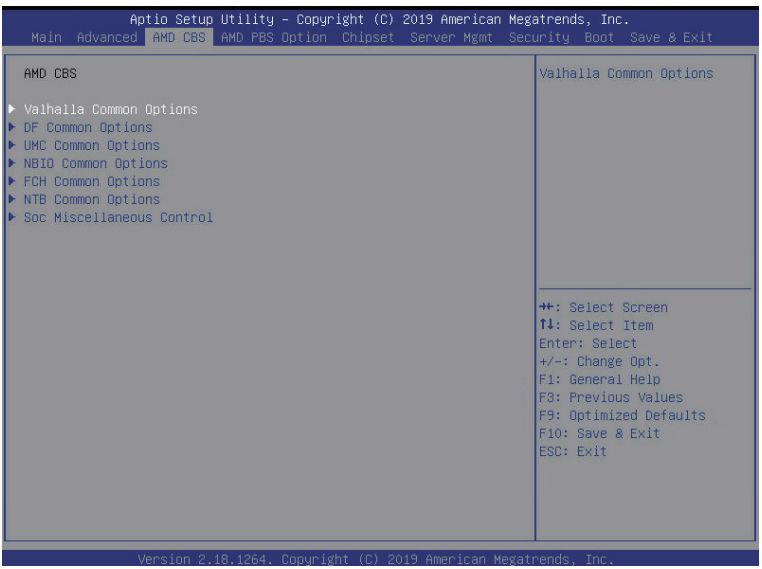
5-2-19 MAC IPv6 Network Configuration



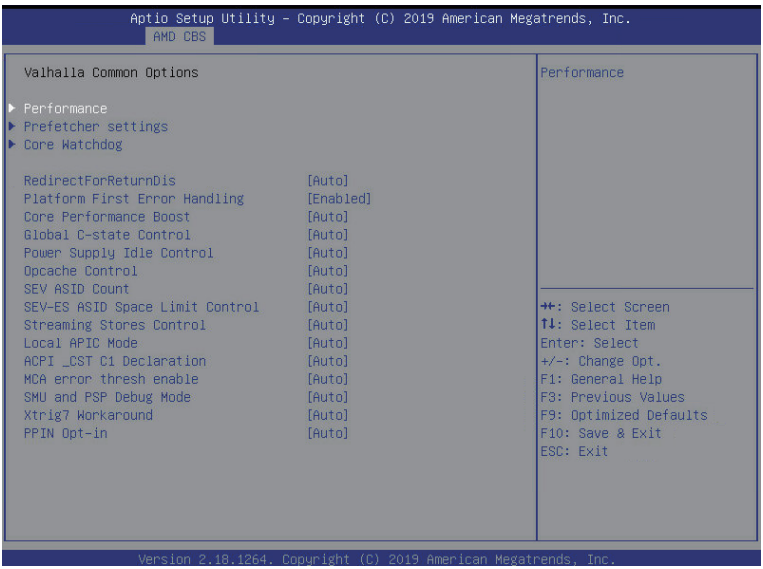
Parameter	Description
Enter Configuration Menu	Press [Enter] for configuration of advanced items. ◆ Interface Name ◆ Interface Type ◆ MAC address ◆ Host address ◆ Route Table ◆ Gateway addresses ◆ DNS addresses ◆ Interface ID – The 64-bit alternative interface ID for the device. The string is colon separated e.g. ff:dd:88:66:cc:1:2:3. ◆ DAD Transmit Count – The number of consecutive Neighbor Solicitaion messages sent while performing Duplicate Address Detection on a tentative address. A value of zero indicates that Duplicate Addres Detection is not performed. ◆ Policy ◆ Save Changes and Exit

5-3 AMD CBS Menu

AMD CBS menu displays submenu options for configuring the CPU-related information that the BIOS automatically sets. Select a submenu item, then press [Enter] to access the related submenu screen.



5-3-1 Valhalla Common Options

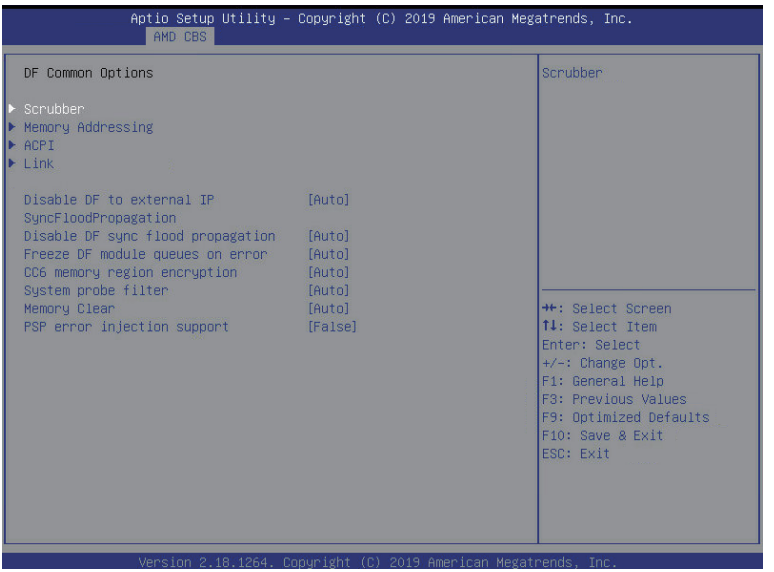


Parameter	Description
Valhalla Common Options	
Performance	Press [Enter] for more options. ◆ Custom Core Pstates – Allows you to accept or decline custom core pstates. When accepted you can disable or customize ceratin pstates. ◆ CCD/Core/Thread Enablement – Allows you to accept or decline enabling CCDs, processor cores and threads. When accepted you can control the number of CCDs to be used, the number of cores to be used, and whether to enable or disable symmetric multithreading.
Prefetcher settings	Press [Enter] for more options. ◆ L1 Stream HW Prefetcher – Option to enable or disable L1 Stream HW Prefetcher – Options available: Disable/Enable/Auto. Default option is **Auto**. ◆ L2 Stream HW Prefetcher – Option to enable or disable L2 Stream HW Prefetcher – Options available: Disable/Enable/Auto. Default option is **Auto**.
Core Watchdog	Press [Enter] for more options. ◆ Core Watchdog Timer Enable – Enable or disable CPU watchdog timer. – Options available: Disable/Enable/Auto. Default option is **Auto**.

Parameter	Description
RedirectForReturnDis	From a workaroud for GCC/C000005 issue for XV Core on CZ A0, setting MSRC001_1029 Decode Configuration (DE_CFG) bit 14 [DecfgNoRdrctForReturns] to 1. Options available: Auto/1/0. Default option is **Auto**.
Platform First Error Warning	Enable/Disable PFEH, cloak individual banks, and mask deferred error interrupts from each bank. Options available: Enabled/Disabled/Auto. Default option is **Enabled**.
Core Performance Boost	Allows you to disable CPB. Options available: Disabled/Auto. Default option is **Auto**.
Global C-State Control	Controls the IO based C-state generation and DF C-states. Options available: Disabled/Enabled/Auto. Default option is **Auto**.
Power Supply Idle Control	Configures the power supply idle control. Options available: Low Current Idle/Typical current Idle/Auto. Default option is **Auto**.
Opcache Control	Enables or disables the Opcache. Options available: Disabled/Enabled/Auto. Default option is **Auto**.
SEV ASID Count	This field specifies the max. valid ASID, which affects the maximum system physical address space. 16TB of physical address space is available for systems that support 253 ASIDs, while 8TB of physical address space is available for systems that support 509 ASIDs. Options available: 253 ASIDs/509 ASIDs/Auto. Default option is **Auto**.
SEV-ES ASID Space Limit Control	Space limit control for SEV-ES ASIDs. Options available: Auto/Manual. Default option is **Auto**.
Streaming Stores Control	Enables or disables the streaming stores functionality. Options available: Disabled/Enabled/Auto. Default option is **Auto**.
Local APIC Mode	Sets the Local APIC mode. Options available: xAPIC/x2APIC/Auto. Default option is **Auto**.
ACPI_CST C1 Decaration	Determines whether or not to declare the C1 state to the OS. Options available: Disabled/Enabled/Auto. Default option is **Auto**.
MCA error thresh enable	Enable MCA error thresholding. Options available: False/True/Auto. Default option is **Auto**.
SMU and PSP Debug Mode	When this option is enabled, specific uncorrected errors detected by the PSP FW or SMU FW will hand and not reset the system. Options available: Disabled/Enabled/Auto. Default option is **Auto**.

Parameter	Description
Xtrig7 Workaround	By default (Auto) the bronze workaround is applied. Bronze workaround: DbReq and PDM function as expected, breakpoint redirect capability compromised. Silver workaround: DbReq, PDM, and breakpoint redirect function as expected, SCAN capability compromised. Options available: Auto/No Workaround/Bronze Workaround/Silver Workaround. Default option is **Auto**.
PPIN Opt-in	Turns on PPIN feature. Options available: Disabled/Enabled/Auto. Default option is **Auto**.

5-3-2 DF Common Options

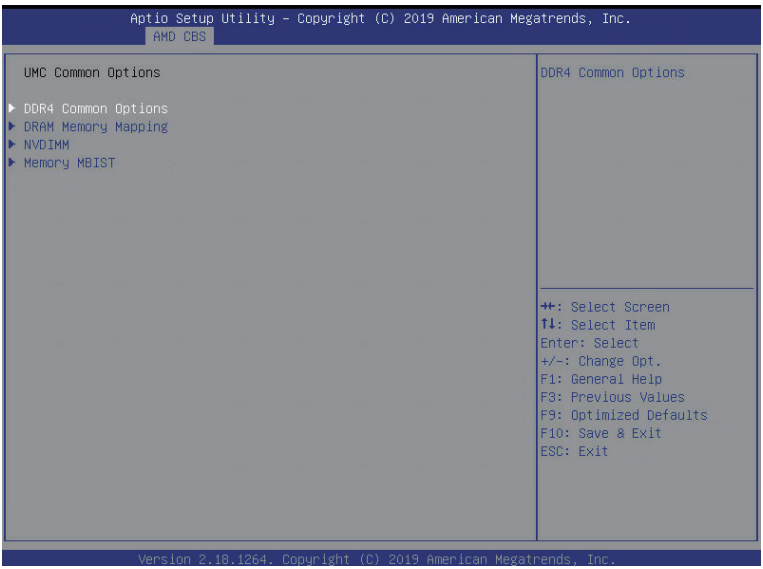


Parameter	Description
Scrubber	Press [Enter] for configuration of advanced items. ◆ DRAM scrub time – Provides a value that is the number of hours to scrub memory. – Options available: Disabled/1 hour/4 hours/8 hours/16 hours/24 hours/48 hours/Auto. Default option is **Auto**. ◆ Poison scrubber control – Allows you to enable or disable poison scrubber control. – Options available: Disabled/Enabled/Auto. Default option is **Auto**. ◆ Redirect scrubber control – Allows you to enable or disable redirect of scrubber control. – Options available: Disabled/Enabled/Auto. Default option is **Auto**. ◆ Redirect scrubber limit – Allows you to set the redirect scrubber limit. – Options available: 2/4/8/Infinite/Auto. Default option is **Auto**.

Parameter	Description
Memory Addressing	Press [Enter] for more options. ◆ NUMA notes per socket – Specifies the number of desired NUMA (Non-uniform Memory Access) notes per socket. Zero will attempt to interleave the two sockets together. – Options available: NPS0/NPS1/NPS2/NPS4/Auto. Default option is **Auto**. ◆ Memory interleaving – Allows for disabling memory interleaving. Note that NUMA nodes per socket will be honored regardless of this setting. – Options available: Disabled/Auto. Default option is **Auto**. ◆ Memory interleaving size – Controls the memory interleaving size. The valid value are AUTO, 256 bytes, 512 bytes, 1Kbytes or 2Kbytes. This determines the starting address of the interleave (bit 8, 9, 10 or 11). – Options available: 256 Bytes/512 Bytes/1 KB/2KB/Auto. Default setting is **Auto**. ◆ 1TB remap – Attempt to remap DRAM out of the space just below the 1TB boundary. The ability to remap depends on DRAM configuration, NPS, and interleaving selection, and may not always be possible. – Options available: Do not remap/Attempt to remap.Auto. Default option is **Auto**. ◆ DRAM map inversion – Inverting the map will cause the highest memory channels to get assigned the lowest addresses in the system. – Options available: Disabled/Enabled/Auto. Default option is **Auto**.
ACPI	Press [Enter] for more options. ◆ ACPI SRAT L3 Cache as NUMA Domain – Enabled: Each CCX in the system will be declared as a separate NUMA domain. – Disabled: Memory Addressing \ NUMA nodes per socket will be declared. – Options available: Disable/Enable/Auto. Default option is **Auto**. ◆ ACPI SLIT Distance Control – Determines how the SLIT distances are declared. – Options available: Manual/Auto. Default option is **Auto**. ◆ ACPI SLIT remote relative distance – Set the remote socket distance for 2P systems as near (2.8) or far (3.2). – Options available: Near/Far/Auto. Default option is **Auto**.

Parameter	Description
Link	Press [Enter] for more options. ◆ GMI encryption control – Control GMI link encryption. – Options available: Disable/Enable/Auto. Default option is **Auto**. ◆ xGMI encryption control – Control xGMI link encryption.Options available: Disable/Enable/Auto. Default option is **Auto**. ◆ CAKE CRC perf bounds control – Control CAKE CRC perf bounds – Options available: Auto/Manual. Default option is **Auto**. ◆ 4-link xGMI max speed – Set 4-link xGMI max speed. – Options available: 10.667Gbps/13Gbps/16Gbps/18Gbps/Auto. Default option is **Auto**. ◆ 3-link xGMI max speed – Set 3-link xGMI max speed. – Options available: 10.667Gbps/13Gbps/16Gbps/18Gbps/Auto. Default option is **Auto**. ◆ xGMI TXEQ Mode – Select XGMI TXEQ/RX vetting Mode. – Options available: TXEQ_Disabled/TXEQ_LAne/TXEQ_Link/TXEQ_RX_Vet/Auto. Default option is **Auto**.
Disable DF to external IP Sync Flood Propagation	Disable SyncFlood to UMC & downstream slaves. Options avaialble: Sync flood disabled/Sync flood enabled/Auto. Default option is **Auto**.
Disable DF sync flood propagation	Enable/Disable DF SyncFlood. Options avaialble: Sync flood disabled/Sync flood enabled/Auto. Default option is **Auto**.
Freeze DF module queues on error	Controls DF PIE Config. Disabling this options sets DF:PIEConfig. Options available: Disable/Enable/Auto. Default option is **Auto**.
CC6 memory region encryption	Control whether or not the CC6 save/restore memory is encrypted. Options available: Disable/Enable/Auto. Default option is **Auto**.
System probe filter	Controls whether or not the probe filter is enabled. Has no effect on parts where the probe filter is fuse disabled. Options available: Disable/Enable/Auto. Default option is **Auto**.
Memory Clear	When this feature is disabled, BIOS does not implement MemClear after memory training (only if non-ECC DIMMs are used). Options available: Disable/Enable/Auto. Default option is **Auto**.
PSP error injection support	Select **True** to enable error injection. Options available: False/True. Default option is **False**.

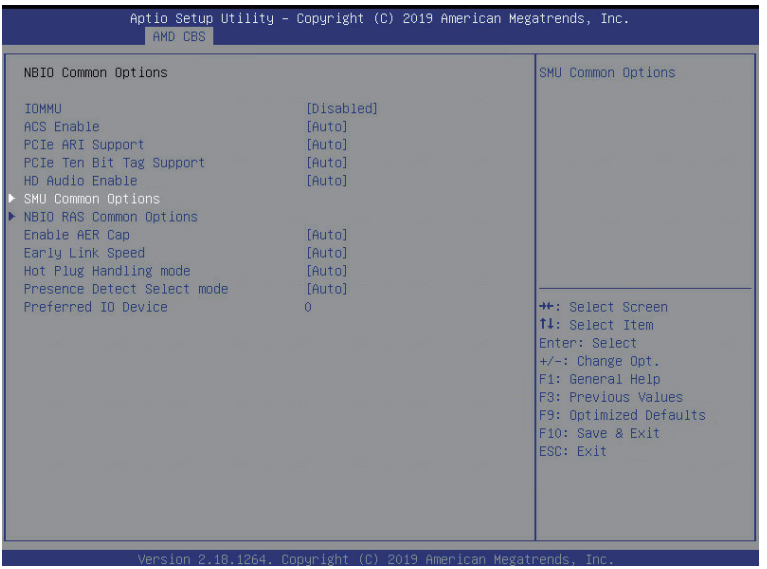
5-3-3 UMC Common Options



Parameter	Description
DDR4 Common Options	Press [Enter] for more options. ◆ Enforce POR – Press [Enter] to configure the enforcement of Plan Of Record (POR) which enables enforcement of POR restrictions for DDR4 frequency and voltage programming. Memory speeds will be capped at Intel guidelines. ◆ DRAM Controller Configuration – Press [Enter] to configure DRAM controller options. ◆ CAD Bus Configuration – Press [Enter] to configure CAD Bus options. ◆ Data Bus configuration – Press [Enter] to configure Data Bus options. ◆ Common RAS – Press [Enter] to configure Common RAS options. ◆ Security – Press [Enter] to configure UMC security options.

Parameter	Description
DRAM Memory Mapping	Press [Enter] for more options ◆ Chipselect Interleaving – Interleave memory blocks across the DRAM chip slects for node 0 – Options available: Disabled/Auto. Default option is **Auto**. ◆ BankGroupSwap – Configures the BankGroupSwap. BankGroupSwap (BGS) is a memory mapping option in AGESA that alters how applications get assigned to physical locations within the memory modules. When this option sets to Auto, it is null. – Options available: Enabled/Disabled/Auto. Default option is **Auto**. ◆ BankGroupSwapAlt – Configures the BankGroupSwapAlt. – Options available: Enabled/Disabled/Auto. Default option is **Auto**. ◆ Address Hash Bank – Enable or disable bank address hashing. – Options available: Disabled/Enabled/Auto. Default option is **Auto**. ◆ Address Hash CS – Enable or disable CS address hashing. – Options available: Auto/Enabled/Disabled. Default option is **Auto**. ◆ Address Hash Rm – Enable or disable RM address hashing. – Options available: Auto/Enabled/Disabled. Default option is **Auto**. ◆ SPD Read Optimization – Enable or disable SPD Read Optimization. Enabled = SPD reads are skipped for Reserved fields and most of upper 256 Bytes, Disabled = read all 512 SPD Bytes. – Options available: Auto/Enabled/Disabled. Default option is **Auto**.
NVDIMM	Press [Enter] for more options.
Memory MBIST	Press [Enter] for more options ◆ MBIST Enable – Enable or disable Memory MBIST. – Options available: Disabled/Enabled. Default option is **Disabled**. ◆ Data Eye – Press [Enter] for more options.

5-3-4 NBIO Common Options



Parameter	Description
NBIO Common Options	
IOMMU	Enable/Disable IOMMU. Options available: Enabled/Disabled. Default setting is **Disabled**.
ACS Enable	AER must be enabled for ACS enable to work. Options available: Enable/Disabled/Auto. Default option is **Auto**.
PCIe ARI Support	Enables Alternative Routing ID Interpretation. Options available: Disable/Enable/Auto. Default option is **Auto**.
PCIe Ten Bit Tag Support	Enables PCIe ten bit tags for supported devices. Auto = Disabled Options available: Disable/Enable/Auto. Default option is **Auto**.
HD Audio Enable	Enables or disables HD Audio. Options available: Enable/Disabled/Auto. Default option is **Auto**.

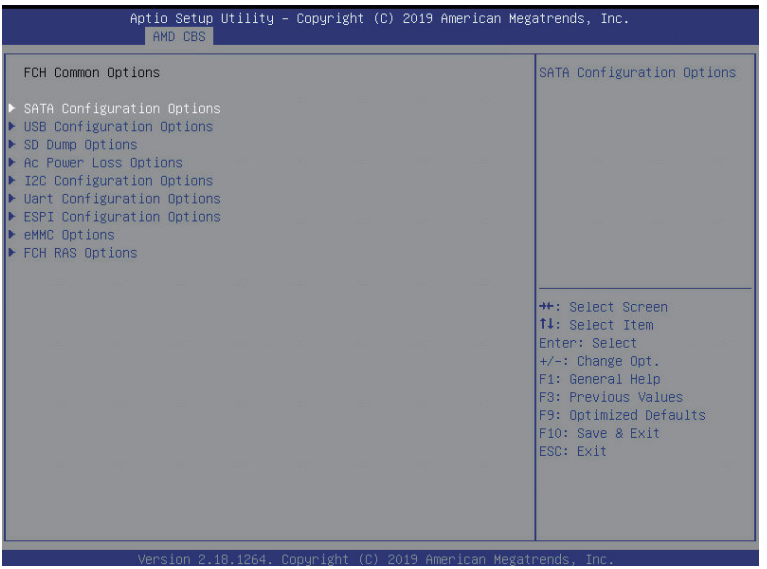
Parameter	Description
SMU Common Options	Press [Enter] for more options. ◆ Determinism Control – Auto = Use the fused determinism, Manual = User can set customized determinism. – Options available: Manual/Auto. Default option is **Manual**. ◆ cTDP Control – Auto = Use the fused TDP, Manual = User can set customized TDP. TDP is used to define the RC thermal model only. – Options available: Manual/Auto. Default option is **Manual**. ◆ Fan Control – Press [Enter] to configure the fan control table. ◆ CLD0_VDDP Control – Manual = User can set customized CLD0_VDDP voltage. – Options available: Auto/Manual. Default option is **Auto**. ◆ EfficiencyModeEn – 0 = use performance optimized CCLK DPM settings, 1 = use power efficiency optimized CCLK DPM settings. – Options available: Auto/Enabled. Default option is **Auto**. ◆ Package Power Limit Control – Auto = Use the fused PPT, Manual = User can set PPT. PPT will be used as the ASIC power limit. – Options available: Manual/Auto. Default option is **Manual**. ◆ xGMI Link Width Control – Auto = Use degault xGMI link width controller, Manual = User can set custom xGMI link width controller settings. – Options available: Manual/Auto. Default option is **Auto**. ◆ APBDIS – 0 = not APBDIS (mission mode), 1 = APBDIS. – Options available: 0/1/Auto. Default option is **Auto**. ◆ DF Cstates – Enable or disable DF C-states. – Options available: Disabled/Enabled/Auto. Default option is **Auto**. ◆ CPPC – Enable or disable CPPC. – Options available: Disabled/Enabled/Auto. Default option is **Auto**. ◆ BoostFmaxEn – Auto = Use degault Fmax, Manual = User can set boost Fmax. – Options available: Manual/Auto. Default option is **Auto**.

Parameter	Description
NBIO RAS Common Options	Press [Enter] for more options. ◆ NBIO RAS Global Control – Options available: Manual/Auto. Default option is **Auto**. ◆ NBIO RAS Control – 0 = Disabled, 1 = MCA, 2 = Legacy. – Options available: Disabled/MCA/Legacy. Default option is **MCA**. ◆ Egress Poison Severity High – Enter a value. Each bit set to 1 enables high severity on the associated IOHC egress port. A bit of 0 indicates low severity. ◆ Egress Poison Severity Low – Enter a value. Each bit set to 1 enables high severity on the associated IOHC egress port. A bit of 0 indicates low severity. ◆ NBIO SyncFlood Generation – This value may be used to mask SyncFlood caused by NBIO RAS options. When set to TRUE SyncFlood from NBIO is masked. When set to FALSE NBIO is capable of generating SyncFlood. – Options available: Enabled/Disabled/Auto. Default option is **Auto**. ◆ NBIO SyncFlood Reporting – This value may be used to enable SyncFlood reporting to APML. When set to TRUE SyncFlood will be reported to APML. When set to FALSE that reporting will be disabled. – Options available: Enabled/Disabled. Default option is **Disabled**. ◆ Egress Poison Mask High – Enter a value. These set the enable mask for masking of errors logged in EGRESS_POISON_STATUS. For each bit set to 1, errors are masked. For each bit set to 0, errors trigger response actions. ◆ Egress Poison Mask Low – Enter a value. These set the enable mask for masking of errors logged in EGRESS_POISON_STATUS. For each bit set to 1, errors are masked. For each bit set to 0, errors trigger response actions. ◆ Uncorrected Converted to Poison Enable Mask High – Enter a value. These set the enable mask for masking of uncorrectable parity errors on internal arrays. For each bit set to 1, a system fatal error event is triggered for UCP errors on arrays associated with that egress port. For each bit set to 0, errors are masked. ◆ Uncorrected Converted to Poison Enable Mask Low – Enter a value. These set the enable mask for masking of uncorrectable parity errors on internal arrays. For each bit set to 1, a system fatal error event is triggered for UCP errors on arrays associated with that egress port. For each bit set to 0, errors are masked.

Parameter	Description
	◆ System Hub Watchdog Timer – Enter a value. This value specifies the timer interval of the SYSHUB watchdog timer in miliseconds. ◆ SLINK Read Response OK – This value specifies whether SLINK read response errors are converted to an Okay response. When this value is set to TRUE, read response errors are converted to Okay responses with data of all FFs. When set to FALSE read response errors are not converted. – Options available: Enabled/Disabled. Default option is Disabled. ◆ SLINK Read Response Error Handling – This value specifies whether SLINK write response errors are converted to an Okay response. When this value is set to 0, write response errors will be logged in the MCA. When set to 1, write response errors will trigger an MCOMMIT error. When this value is set to 2, write response errors are converted to Okay responses. – Options available: Enabled/Trigger MCOMMIT Error/Log Errors in MCA. Default option is Log Errors in **MCA**.
NBIO RAS Common Options (continued)	◆ Log Poison Data from SLINK – This value specifies whether poison data propogated from SLINK will generate a deferred error. When this value is set to TRUE, deferred errors are enabled. When set to FALSE, errors are not generated. – Options available: Enabled/Disabled. Default option is **Disabled**. ◆ PCIe Aer Reporting Mechanism – This value selects the method of reporting AER errors from PCI Express. A value of 0 indicates that the hardware will report the error through MCA. A value of 1 allows OS First handling of the errors through generation of a system control interrupt (SCI). A value of 2 provides for Firmware First handling of errors through generation of a system management interrupt (SMI). – Options available: OS First/MCA/Auto. Default option is **Auto**. ◆ Edpc Control – (0) Disabled; (1) Enabled; (3) Auto. – Options available: Disabled/Enabled/Auto. Default option is **Disabled**. ◆ NBIO Poison Consumption – Options available: Auto/Enabled/Disabled. Default option is **Auto**.

Parameter	Description
NBIO RAS Common Options (continued)	◆ Sync Flood on PCIe Fatal Error – When 'Sync Flood on PCIe Fatal Error' is True, PcdAmdPcieSyncFloodOnFatal should be set to True. When 'Sync Flood on PCIe Fatal Error' is False, PcdAmdPcieSyncFloodOnFatal should be set to False. When 'Sync Flood on PCIe Fatal Error' is Auto, PcdAmdPcieSyncFloodOnFatal should retain its AGESA default. – Options available: Auto/True/False. Default option is **Auto**.
Enable AER Cap	Enables Advanced Error Reporting Capabilty. Options available: Enable/Disabled/Auto. Default option is **Auto**.
Early Link Speed	Sets Early Link Speed. Options available: Auto/Gen1/Gen2. Default option is **Auto**.
Hot Plug Handling mode	Controls the Hot Plug Handling mode. Options available: A0 Mode/OS First (No Error Handling)/OS First (Error Handling - Not Implementd/Firmware First (Not Implemented)/Auto. Default option is **Auto**.
Presence Detect Select mode	Controls the Presence Detect Select mode. Options available: OR/And/Auto. Default option is **Auto**.
Preferred IO Device	Enter a value for the preferred IO device. [23:16] Bus Number [15:8] Dev Number [7:0] Fun Number

5-3-5 FCH Common Options

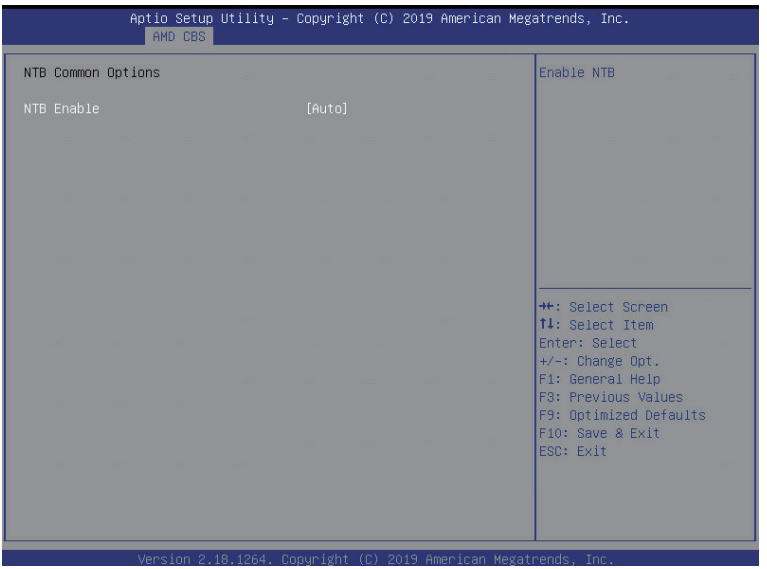


Parameter	Description
FCH Common Options	
SATA Configuration Options	◆ SATA Enable – Enable or disable OnChip SATA controller. – Options available: Disabled/Enabled/Auto. Default setting is **Auto**. ◆ SATA RAS Support – Enable or disable SATA RAS support. – Options available: Disabled/Enabled/Auto. Default setting is **Auto**. ◆ Sata Disabled AHCI Prefetch Function – Enable or disable Sata Disabled AHCI Prefetch Function. – Options available: Disabled/Enabled/Auto. Default setting is **Auto**. ◆ Aggressive SATA Device Sleep Port 0 – Options available: Disabled/Enabled/Auto. Default setting is **Auto**. ◆ Aggressive SATA Device Sleep Port 1 – Options available: Disabled/Enabled/Auto. Default setting is **Auto**.

Parameter	Description
USB Configuration Options	Press [Enter] for more options. ◆ XHCI Controller0 Enable – Enable or disable USB3 controller. – Options available: Enabled/Disabled/Auto. Default setting is **Auto**. ◆ XHCI Controller1 Enable – Enable or disable USB3 controller. – Options available: Enabled/Disabled/Auto. Default setting is **Auto**. ◆ USB ecc SMI Enable – Options available: Enabled/Off/Auto. Default setting is **Auto**. ◆ MCM USB enable – Press [Enter] for advanced configurations.
SD Dump Options	Press [Enter] for more options. ◆ SD Configuration Mode – Select SD Mode. – Options available: SD Dump disabled/SD Dump Enabled. Default setting is **SD Dump disabled**.
AC Power Loss Options	Press [Enter] for more options. ◆ AC Loss Control – Select AC Loss Control Method. – Options available: Power Off/Power On/Last State. Default setting is **Last State**.
I2C Configuration Options	Press [Enter] for more options. ◆ I2C 0/1/2/3/4/5 Enable – Enable or disable I2C 0/1/2/3/4/5. – Options available: Disabled/Enabled/Auto. Default setting is **Auto**.
Uart Configuration Options	Press [Enter] for more options. ◆ Uart 0 Enable – Uart 0 has no HW FC if Uart 2 is enabled. – Options available: Disabled/Enabled/Auto. Default setting is **Auto**. ◆ Uart 1 Enable – Uart 1 has no HW FC if Uart 3 is enabled. – Options available: Disabled/Enabled/Auto. Default setting is **Auto**. ◆ Uart 2 Enable (no HW FC) – Options available: Disabled/Enabled/Auto. Default setting is **Auto**. ◆ Uart 3 Enable (no HW FC) – Options available: Disabled/Enabled/Auto. Default setting is **Auto**.
ESPI Configuration Options	Press [Enter] for more options. ◆ ESPI Enable – Options available: Disabled/Enabled/Auto. Default setting is **Auto**.

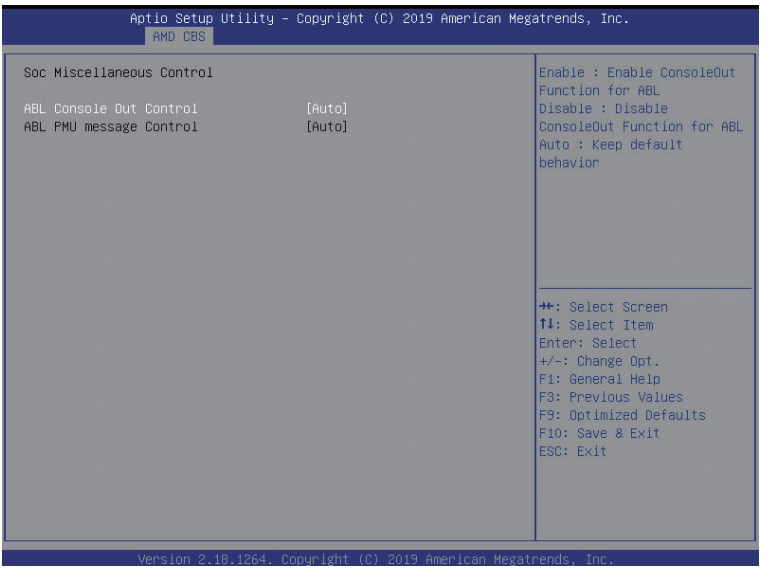
Parameter	Description
eMMC Options	Press [Enter] for more options. ◆ eMMC/SD Configure – Options available: Disabled/SD Normal Speed/SD High Speed/SD UHSI-SDR50/SD UHSI-DDR50/SDUHSI-SDR104/eMMC Emmc Backward Compatibility/eMMC High Speed SDR/eMMC High Speed DDR/eMMC HS200/eMMCHS400/eMMC HS300/Auto. Default setting is **Auto**. ◆ Driver Type – BIOS will select MS driver for SD selections. – Options available: AMD eMMC Driver/MS Driver/Auto. Default setting is **Auto**. ◆ D3 Cold Support – Options available: Disabled/Enabled/Auto. Default setting is **Auto**. ◆ eMMC Boot – Options available: Disabled/Enabled/Auto. Default setting is **Auto**.
FCH RAS Options	Press [Enter] for more options. ◆ ALink RAS Support – Options available: Disabled/Enabled/Auto. Default setting is **Auto**. ◆ Reset after sync flood – Enable AB to forward downstream sync-flood message to system controller. – Options available: Disabled/Enabled/Auto. Default setting is **Auto**.

5-3-6 NTB Common Options



Parameter	Description
NTB Common Options	
NTB Enable	Enable or disable OnChip SATA controller. Options available: Auto/Enable. Default setting is **Auto**.

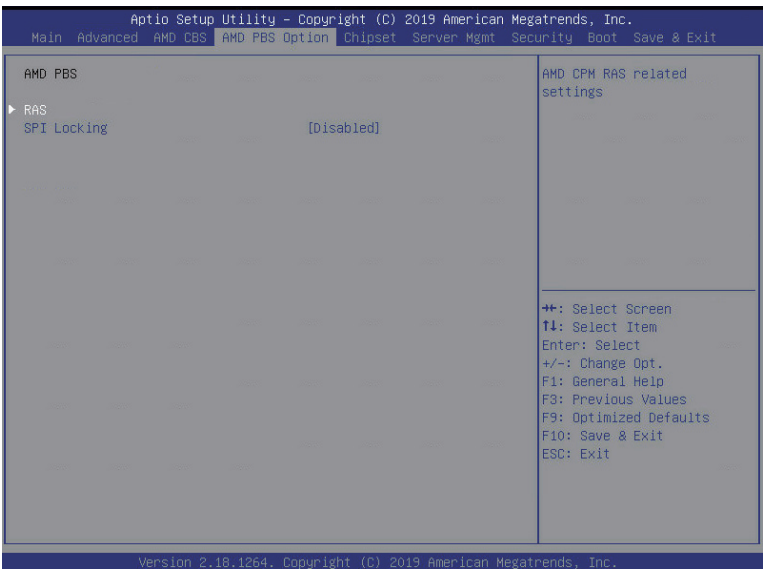
5-3-7 SOC Miscellaneous Control



Parameter	Description
Soc Miscellaneous Control	
ABL Console Out Control	Enable = Enable ConsoleOut Function for ABL Disable = Disable ConsoleOut Function for ABL Auto = Keep default behavior Options available: Disable/Enable/Auto. Default setting is **Auto**.

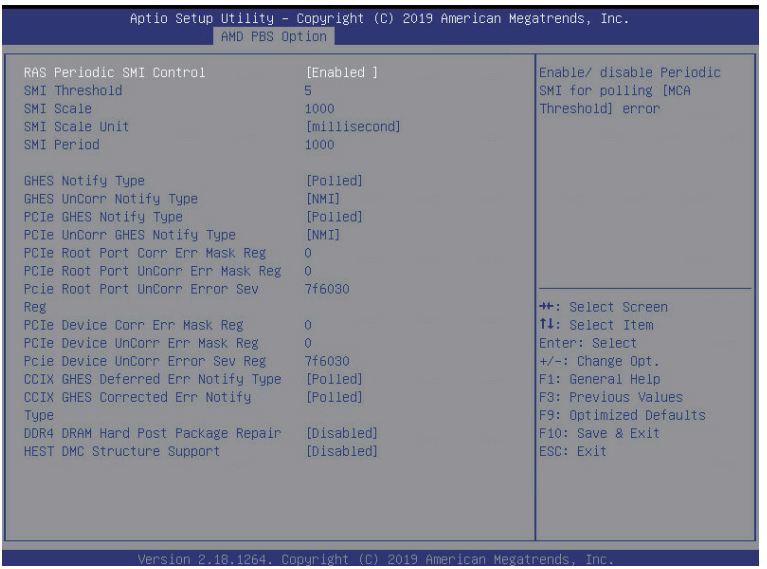
5-4 AMD PBS Option Menu

AMD PBS Option menu displays submenu options for configuring the function of AMD PBS. Select a submenu item, then press [Enter] to access the related submenu screen.



Parameter	Description
AMD PBS	
RAS	Press [Enter] for advanced configurations.
SPI Locking	Enable or disable SPI Locking for protect ROM part. Options Available: Enabled/Disabled. Default option is **Disabled**.

5-4-1 RAS

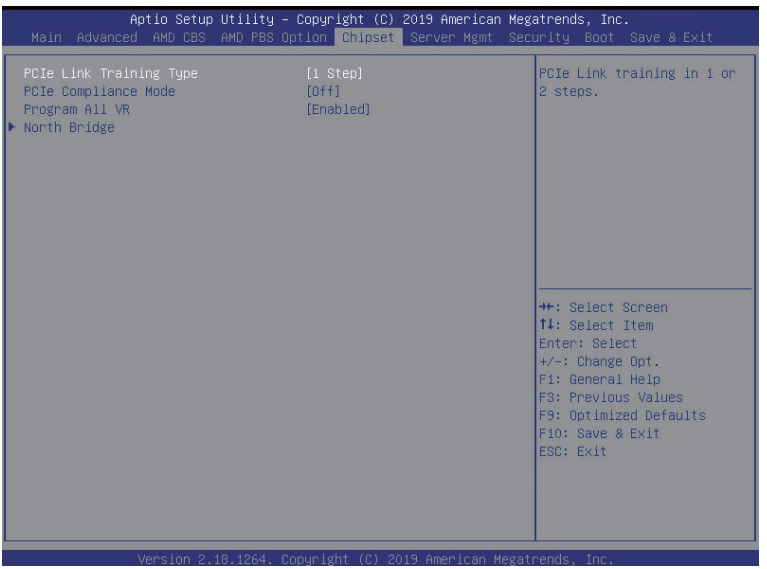


Parameter	Description
RAS Periodic SMI Control	Enable or disable Periodic SMI for polling [MCA Threshold] error. Options Available: Disabled/Enabled. Default option is **Enabled**.
SMI Threshold	Enter a value. Limits the number of [MCA Threshold and Deferred Error SMI source] per a unit of time (Defined by [SMI Scale]). Default value is **5 dec interrupts**.
SMI Scale	Enter a value. Defines the time scale. Default value is **1000 dec**.
SMI Scale Unit	Defines the unit of time scale. Options available: millisecond/second/minute. Default option is **millisecond**.
SMI Period	Enter a value. Defines the polling interval in milliseconds. Default option is **1000 dec**. Maximum value is 32767 dec. 0 = disable.
GHES Notify Type	Notification type for deferred/corrected errors. Options Available: Polled/SCI. Default option is **Polled**.
GHES UnCorr Notify Type	Notification type for uncorrected errors. Options Available: Polled/NMI. Default option is **NMI**.
PCIe GHES Notify Type	Notification type for PCIe corrected errors. Options Available: Polled/SCI. Default option is **Polled**.

Parameter	Description
PCIe UnCorr GHES Notify Type	Notification type for PCIe uncorrected errors. Options Available: Polled/NMI. Default option is **NMI**.
PCIe Root Port Corr Err Mask Reg	Enter a value. Intialize the PCIe AER Corrected Error Mask register of Root Port.
PCIe Root Port UnCorr Err Mask Reg	Enter a value. Intialize the PCIe AER Uncorrected Error Mask register of Root Port.
PCIe Root Port UnCorr Error Sev Reg	Enter a value. Intialize the PCIe AER Uncorrected Error Severity register of Root Port.
PCIe Device Corr Err Mask Reg	Enter a value. Intialize the PCIe AER Corrected Error Mask register of PCIe Device.
PCIe Device UnCorr Err Mask Reg	Enter a value. Intialize the PCIe AER Uncorrected Error Mask register of PCIe Device.
PCIe Device UnCorr Error Sev Reg	Enter a value. Intialize the PCIe AER Uncorrected Error Severity registers of PCIe Device.
CCIX GHES Deferred Err Notify Type	Notification type for CCIX deferred errors. Options Available: Polled/SCI. Default option is **Polled**.
CCIX GHES Corrected Err Notify Type	Notification type for CCIX corrected errors. Options Available: Polled/SCI. Default option is **Polled**.
DDR4 DRAM Hard Post Package Repair	This feature allows spare DRAM rows to replace malfunctioning rows via an in-field repair mechanism. Options Available: Disabled/Enabled. Default option is **Disabled**.
HEST DMC Structure Support	HEST DMC (Deferred Machine Check) Structure Support. Options Available: Disabled/Enabled. Default option is **Disabled**.

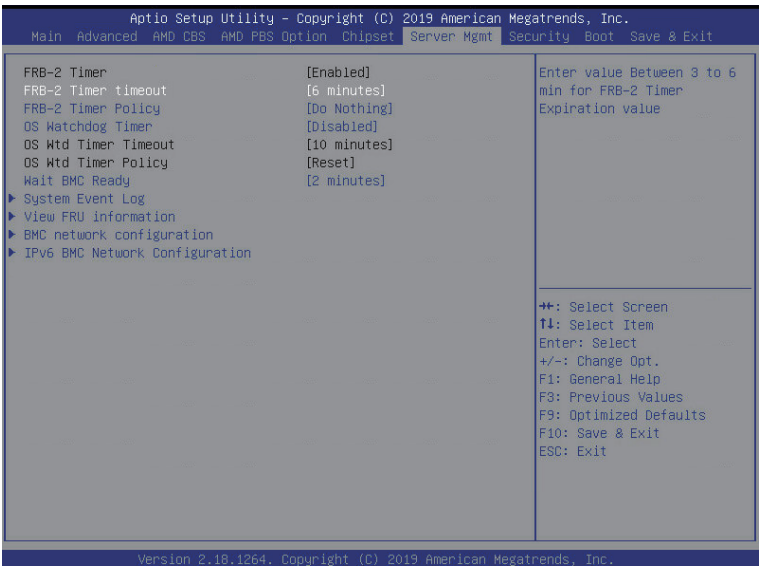
5-5 Chipset Setup Menu

Chipset Setup menu displays submenu options for configuring the function of the North Bridge. Select a submenu item, then press [Enter] to access the related submenu screen.



Parameter	Description
PCIe Link Training Type	PCIe Link training in 1 or 2 steps. Options available: 1 Step/2Step. Default setting is **1 Step**.
PCIe Compliance Mode	Options available: On/Off. Default setting is **Off**.
Program All VR	Enables or disables program all VR on MB. Options available: Disabled/Enabled. Default setting is **Enabled**.
North Bridge	Press [Enter] for more information on the North Bridge.

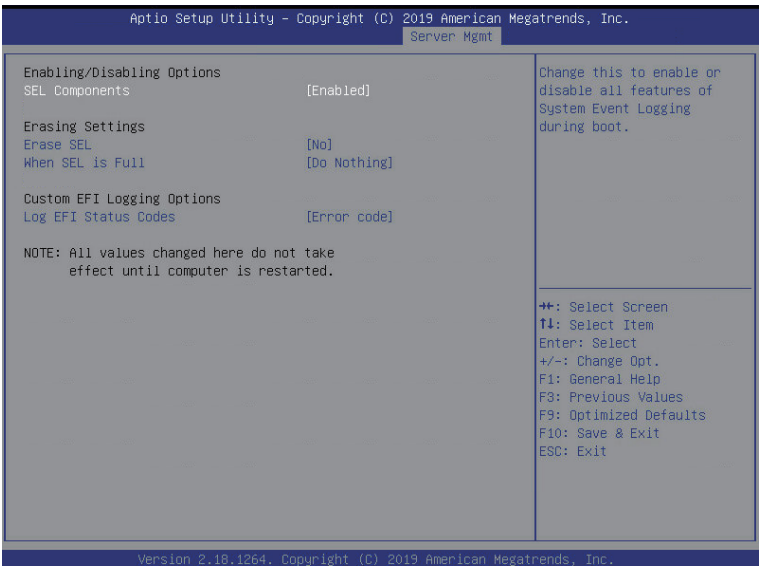
5-6 Server Management Menu



Parameter	Description
FRB-2 Timer	FRB-2 timer (POST timer).
FRB-2 Timer timeout	Configure the FRB2 Timer timeout. Options available: 3 minutes/4 minutes/5 minutes/6 minutes. Default setting is **6 minutes**. (NOTE) This item is configurable when FRB-2 Timer is set to Enabled.
FRB-2 Timer Policy	Configure the FRB2 Timer policy. Options available: Do Nothing/Reset/Power Down. Default setting is **Do Nothing**. (NOTE) This item is configurable when FRB-2 Timer is set to Enabled.
OS Watchdog Timer	Enable/Disable OS Watchdog Timer function. Options available: Enabled/Disabled. Default setting is **Disabled**.
OS Wtd Timer Timeout	Configure OS Watchdog Timer. Options available: 5 minutes/10 minutes/15 minutes/20 minutes. Default setting is **10 minutes**. (NOTE) This item is configurable when OS Watchdog Timer is set to Enabled.
OS Wtd Timer Policy	Configure OS Watchdog Timer Policy. Options available: Reset/Do Nothing/Power Down. Default setting is **Reset**. (NOTE) This item is configurable when OS Watchdog Timer is set to Enabled.
Wait BMC Ready	Configure time to wait BMC ready. Options available: Disabled/2 minutes/4 minutes/6 minutes. Default setting is **2 minutes**.
System Event Log	Press [Enter] to configure advanced items.

Parameter	Description
View FRU Information	Press [Enter] to view the advanced items.
BMC network configuration	Press [Enter] to configure advanced items.
IPv6 BMC Network Configuration	Press [Enter] to configure advanced items.

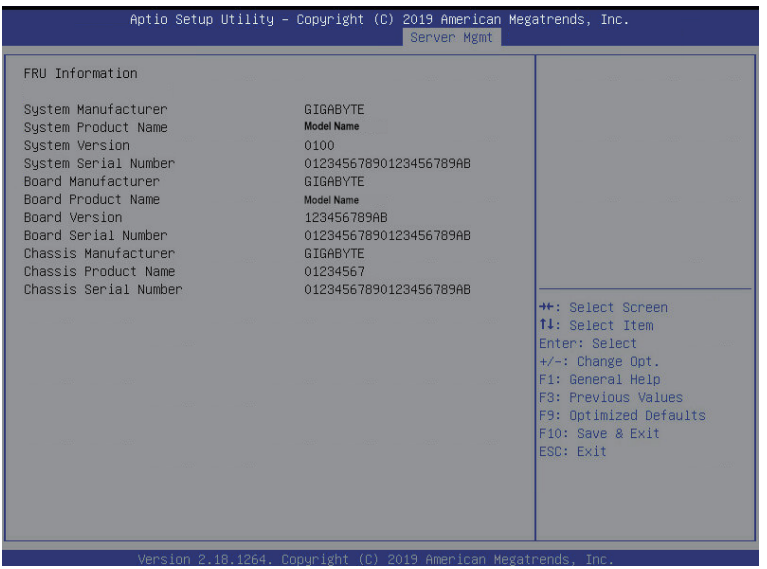
5-6-1 System Event Log



Parameter	Description
Enabling / Disabling Options	
SEL Components	Change this item to enable or disable all features of System Event Logging during boot. Options available: Enabled/Disabled. Default setting is **Enabled**.
Erasing Settings	
Erasing SEL	Choose options for erasing SEL. Options available: No/Yes, On next reset/Yes, On every reset. Default setting is **No**.
When SEL is Full	Choose options for reactions to a full SEL. Options available: Do Nothing/Erase Immediately. Default setting is **Do Nothing**.
Custom EFI Logging Options	
Log EFI Status Codes	Enable/Disable the logging of EFI Status Codes (if not already converted to legacy). Options available: Disabled/Both/Error code/Progress code. Default setting is **Error code**.

5-6-2 View FRU Information

The FRU page is a simple display page for basic system ID information, as well as System product information. Items on this window are non-configurable.



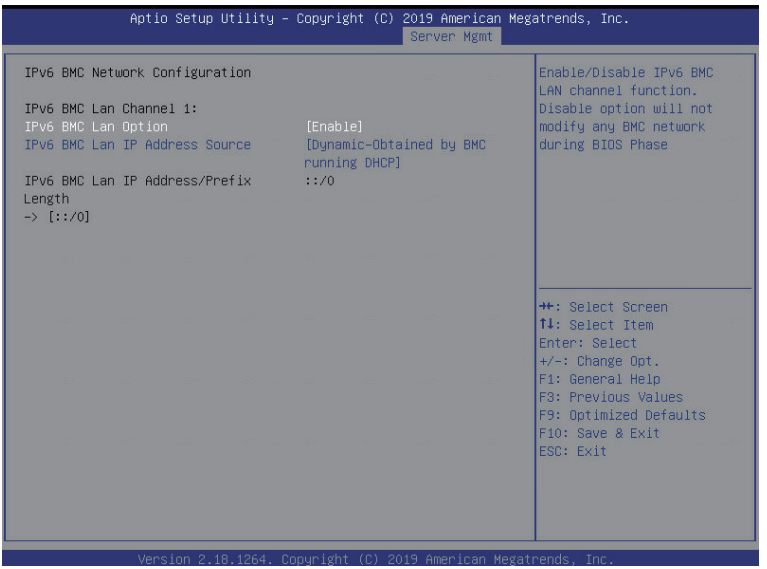
(Note) The model name will vary depends on the product you purchased.

5-6-3 BMC Network Configuration



Parameter	Description
BMC network configuration	
Lan Channel 1	
Configuration Address source	Select to configure LAN channel parameters statically or dynamically (DHCP). Do nothing option will not modify any BMC network parameters during BIOS phase. Options available: Unspecified/Static/DynamicBmcDhcp. Default setting is **DynamicBmcDhcp**.
Station IP address	Displays IP Address information.
Subnet mask	Displays Subnet Mask information.
Router IP address	Displays the Router IP Address information.
Station MAC address	Displays the MAC Address information.
Real-time synchronize BMC network parameter values	Press [Enter] to synchronize the BMC network parameter values.

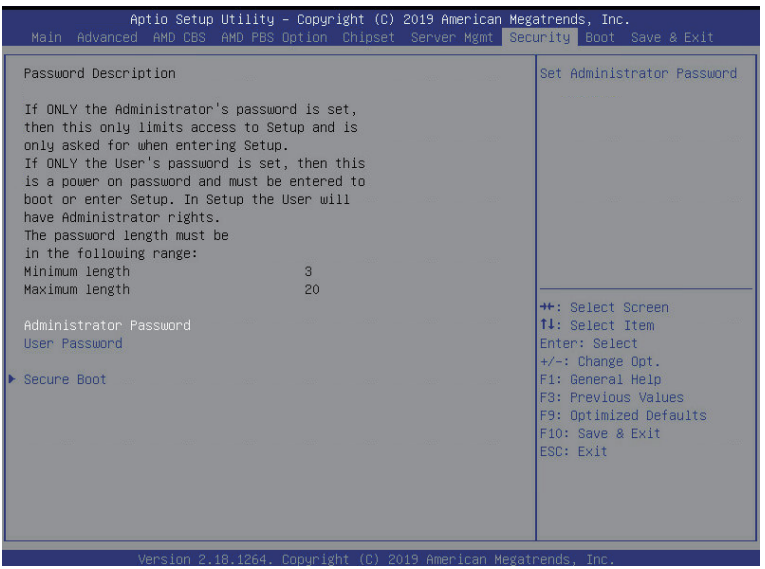
5-6-4 IPv6 BMC Network Configuration



Parameter	Description
IPv6 BMC Network Configuration	
IPv6 BMC Lan Channel 1	
IPv6 BMC Lan Option	Enable/Disable IPv6 BMC LAN channel function. When this item is disabled, the system will not modify any BMC network during BIOS phase. Options available: Unspecified/Disable/Enable. Default setting is **Enable**.
IPv6 BMC Lan IP Address Source	Select to configure LAN channel parameters statically or dynamically (by BIOS or BMC). Options available: Unspecified/Static/Dynamic-Obtained by BMC running DHCP. Default setting is **Dynamic-Obtained by BMC running DHCP**.
IPv6 BMC Lan IP Address/ Prefix Length	Check if the IPv6 BMC LAN IP address matches those displayed on the screen.

5-7 Security Menu

The Security menu allows you to safeguard and protect the system from unauthorized use by setting up access passwords.



There are two types of passwords that you can set:

- Administrator Password

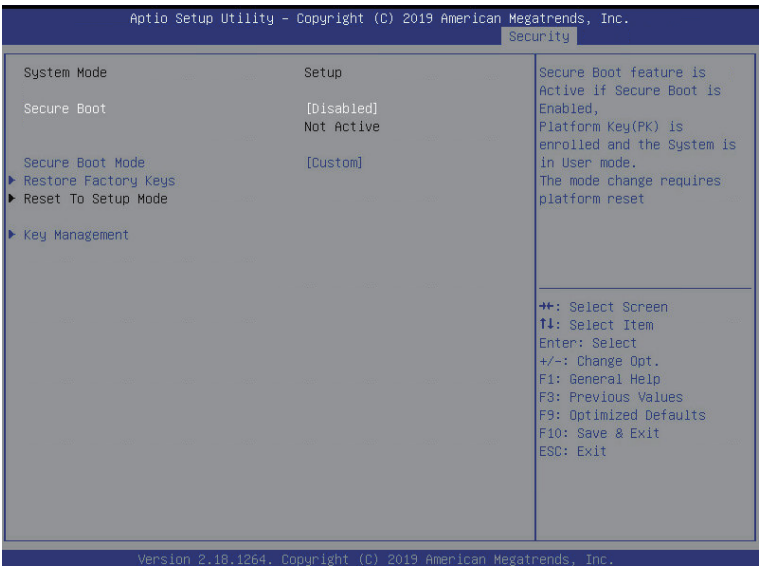
  Entering this password will allow the user to access and change all settings in the Setup Utility.

- User Password

  Entering this password will restrict a user's access to the Setup menus. To enable or disable this field, a Administrator Password must first be set. A user can only access and modify the System Time, System Date, and Set User Password fields.

Parameter	Description
Administrator Password	Press [Enter] to configure the administrator password.
User Password	Press [Enter] to configure the user password.
Secure Boot	Press [Enter] to configure advanced items.

5-7-1 Secure Boot



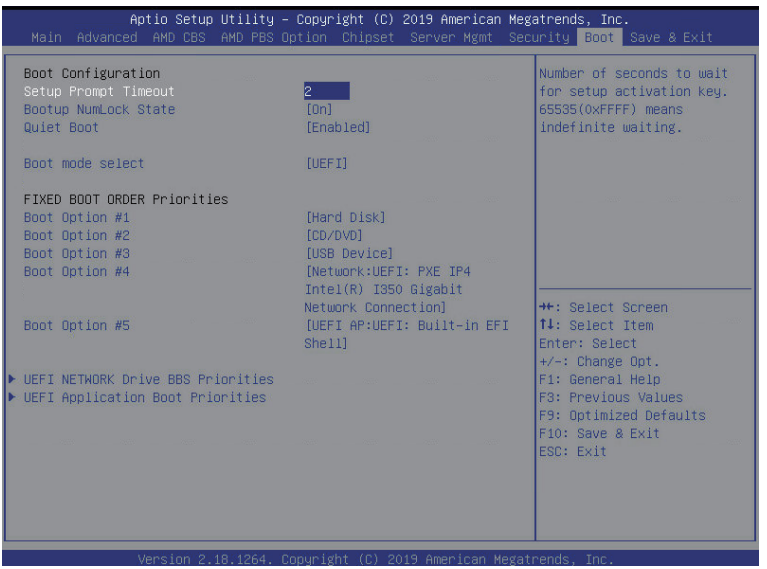
Parameter	Description
System Mode	Displays the system is in User mode or Setup mode.
Secure Boot	Enables/Disables Secure Boot. The mode change requires a platform reset. Options available: Disabled/Enabled. Default setting is **Disabled**.
Secure Boot Mode(Note)	Secure Boot requires all the applications that are running during the booting process to be pre-signed with valid digital certificates. This way, the system knows all the files being loaded before Windows loads and gets to the login screen have not been tampered with. When set to Standard, it will automatically load the Secure Boot keys form the BIOS databases. When set to Custom, you can customize the Secure Boot settings and manually load its keys from the BIOS database. Options available: Standard/Custom. Default setting is **Custom**.
Restore Factory Keys	Forces the system to user mode and installs factury default Secure Boot key database.
Key Management	Press [Enter] to configure advanced items. **Please note that this item is configurable when Secure Boot Mode is set to Custom.**

(Note) Advanced items prompt when this item is set to **Custom**.

Parameter	Description
Key Management (continued)	◆ Factory Key Provision – Installs factory default Secure Boot keys after the platform resets and the system is in Setup Mode. – Options available: Disabled/Enabled. Default setting is Disabled. ◆ Restore Factory Keys – Installs factory default Secure Boot key databases. It will force the system in User Mode. – Options available: Yes/No. ◆ Enroll Efi Image – Press [Enter] to enroll SHA256 hash of the binary into Authorized Signature Database (db). ◆ Restore DB defaults – Press [Enter] to restore DB variable to factory defaults. – Options available: Yes/No. ◆ Secure Boot variable – Displays the current status of the variables used for secure boot. ◆ Platform Key (PK) – Displays the current status of the Platform Key (PK). – Press [Enter] to configure a new PK. – Options available: Set Update. ◆ Key Exchange Keys (KEK) – Displays the current status of the Key Exchange Key Database (KEK). – Press [Enter] to configure a new KEK or load additional KEK from storage devices. – Options available: Set Update/Append. ◆ Authorized Signatures (DB) – Displays the current status of the Authorized Signature Database. – Press [Enter] to configure a new DB or load additional DB from storage devices. – Options available: Set Update/Append. ◆ Forbidden Signatures (DBX) – Displays the current status of the Forbidden Signature Database. – Press [Enter] to configure a new dbx or load additional dbx from storage devices. – Options available: Set Update/Append. ◆ Authorized TimeStamps (DBT) – Displays the current status of the Authorized TimeStamps Database. – Press [Enter] to configure a new DBT or load additional DBT from storage devices. – Options available: Set Update/Append. ◆ OsRecovery Signatures – Displays the current status of the OsRecovery Signature Database. – Press [Enter] to configure a new OsRecovery Signature or load additional OsRecovery Signature from storage devices. – Options available: Set Update/Append.

5-8 Boot Menu

The Boot menu allows you to set the drive priority during system boot-up. BIOS setup will display an error message if the legacy drive(s) specified is not bootable.

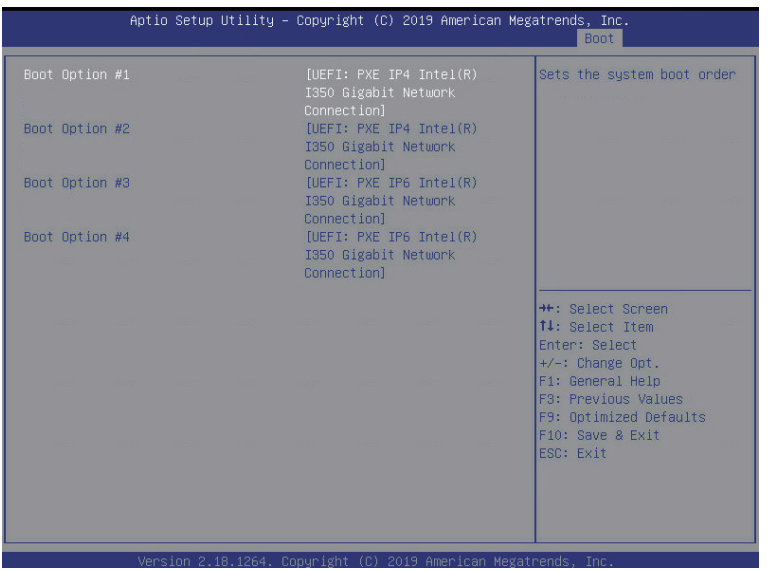


Parameter	Description
Boot Configuration	
Setup Prompt Timeout	Number of seconds to wait for setup activation key. 65535 (0xFFFF) means indefinite waiting. Press the numeric keys to input the desired values.
Bootup NumLock State	Enable/Disable the Bootup NumLock function. Options available: On/Off. Default setting is **On**.
Quiet Boot	Enable/Disable showing the logo during POST. Options available: Disabled/Enabled. Default setting is **Enabled**.
Boot mode select	Selects the boot mode. Options available: LEGACY/UEFI. Default setting is **UEFI**.
FIXED BOOT ORDER Priorities	
Boot Option #1 / #2 / #3 / #4 / #5	Press [Enter] to configure the boot priority. By default, the server searches for boot devices in the following sequence: 1. Hard drive. 2. CD-COM/DVD drive. 3. USB device. 4. Network. 5. UEFI.

Parameter	Description
UEFI Network Drive BBS Priorities	Press [Enter] to configure the boot priority.
UEFI Application Boot Priorities	Press [Enter] to configure the boot priority.

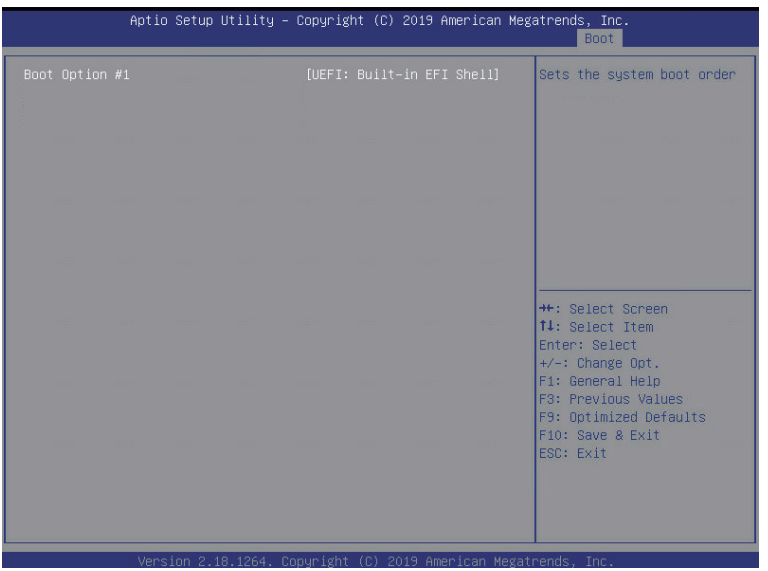
5-8-1 UEFI NETWORK Drive BBS Priorities

The UEFI network drive BBS priorities submenu allows you to specify the boot device priority from the available UEFI network drives during system boot-up. BIOS setup will display an error message if the legacy drive(s) specified is not bootable.



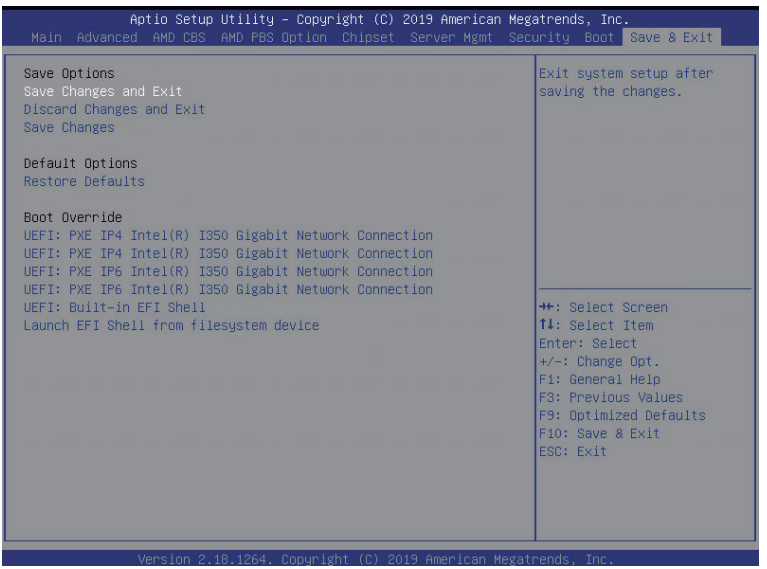
5-8-2 UEFI Application Boot Priorities

The UEFI application boot priorities submenu allows you to specify the boot device priority from the available UEFI applications during system boot-up. BIOS setup will display an error message if the legacy drive(s) specified is not bootable.



5-9 Save & Exit Menu

The Exit menu displays the various options to quit from the BIOS setup. Highlight any of the exit options then press [Enter].



Parameter	Description
Save Options	
Save Changes and Exit	Saves changes made and closes the BIOS setup. Options available: Yes/No.
Discard Changes and Exit	Discards changes made and exits the BIOS setup. Options available: Yes/No.
Save Changes	Save changes done so far to any of the setup options. Options available: Yes/No.
Default Options	
Restore Defaults	Loads the default settings for all BIOS setup parameters. Setup Defaults are quite demanding in terms of resources consumption. If you are using low-speed memory chips or other kinds of low-performance components and you choose to load these settings, the system might not function properly. Options available: Yes/No.
Boot Override	Press [Enter] to configure the device as the boot-up drive.
Launch EFI Shell from filesystem device	Attempts to Launch EFI Shell application (Shell.efi) from one of the available filesystem devices.

5-10 ABL POST Codes

5-10-1 StartProcessorTestPoints

Entry used for range testing for @b Processor related TPs	0xE000

5-10-2 Memory test points

Memory structure initialization (Public interface)	0xE001
SPD Data processing (Public interface)	0xE002
Memory configuration (Public interface) Phase 1	0xE003
DRAM initialization	0xE004
ProcMemSPDChecking	0xE005
ProcMemModeChecking	0xE006
Speed and TCL configuration	0xE007
ProcMemSpdTiming	0xE008
ProcMemDramMapping	0xE009
ProcMemPlatformSpecificConfig	0xE00A
ProcMemPhyCompensation	0xE00B
ProcMemStartDcts	0xE00C
ProcMemBeforeDramInit (Public interface)	0xE00D
ProcMemPhyFenceTraining	0xE00E
ProcMemSynchronizeDcts	0xE00F
ProcMemSystemMemoryMapping	0xE010
ProcMemMtrrConfiguration	0xE011
ProcMemDramTraining	0xE012
ProcMemBeforeAnyTraining(Public interface)	0xE013

5-10-3 PMU Test Points

ABL Mem - PMU - Before PMU Firmware load	0xE014
ABL Mem - PMU - After PMU Firmware load	0xE015
ABL Mem - PMU Populate SRAM Timing	0xE016
ABL Mem - PMU Populate SRAM Config	0xE017
ABL Mem - PMU Write SRAM Msg Block	0xE018
ABL Mem - Wait for Phy Cal Complete	0xE019
ABL Mem - Phy Cal Complete	0xE01A
ABL Mem - PMU Start	0xE01B
ABL Mem - PMU Started	0xE01C
ABL Mem - PMU Waiting for Complete	0xE01D
ABL Mem - PMU Stage Dec Init	0xE01E
ABL Mem - PMU Stage Training Wr Lvl	0xE01F
ABL Mem - PMU Stage Training Rx En	0xE020
ABL Mem - PMU Stage Training Rd Dqs	0xE021
ABL Mem - PMU Stage Training Rd 2D	0xE022

ABL Mem - PMU Stage Training Wr 2D	0xE023
ABL Mem - PMU Queue Empty	0xE024
ABL Mem - PMU US message Start	0xE025
ABL Mem - PMU US message End	0xE026
ABL Mem - PMU Complete	0xE027
ABL Mem - PMU - After PMU Training	0xE028
ABL Mem - PMU - Before Disable PMU	0xE029

5-10-4 Original Post Code

ProcMemTransmitDqsTraining	0xE02A
ABL Mem - Start write sweep	0xE02B
ABL Mem - Set Transmit DQ delay	0xE02C
ABL Mem - Write test pattern	0xE02D
ABL Mem - Read Test pattern	0xE02E
ABL Mem - Compare Test pattern	0xE02F
ABL Mem - Update results	0xE030
ABL Mem - Start Find passing window	0xE031
ABL Mem - ProcMemMaxRdLatencyTraining	0xE032
ABL Mem - Start sweep	0xE033
ABL Mem - Set delay	0xE034
ABL Mem - Write test pattern	0xE035
ABL Mem - Read Test pattern	0xE036
ABL Mem - Compare Test pattern	0xE037
ABL Mem - Online Spare init	0xE038
ABL Mem - Chip select Interleave Init	0xE039
ABL Mem - Node Interleave Init	0xE03A
ABL Mem - Channel Interleave Init	0xE03B
ABL Mem - ECC initialization	0xE03C
ABL Mem - Platform Specific Init	0xE03D
ABL Mem - Before callout for "AgesaReadSpd"	0xE03E
ABL Mem - After callout for "AgesaReadSpd"	0xE03F
ABL Mem - Before optional callout "AgesaHookBeforeDramInit"	0xE040
ABL Mem - After optional callout "AgesaHookBeforeDramInit"	0xE041
ABL Mem - Before optional callout "AgesaHookBeforeDQSTraining"	0xE042
ABL Mem - After optional callout "AgesaHookBeforeDQSTraining"	0xE043
ABL Mem - Before optional callout "AgesaHookBeforeDramInit"	0xE044
ABL Mem - After optional callout "AgesaHookBeforeDramInit"	0xE045
ABL Mem - After MemDataInit	0xE046
ABL Mem - Before InitializeMCT	0xE047
ABL Mem - Before LV DDR3	0xE048
ABL Mem - Before InitMCT	0xE049

ABL Mem - Before OtherTiming	0xE04A
ABL Mem - Before UMAMemTyping	0xE04B
ABL Mem - Before SetDqsEccTmgs	0xE04C
ABL Mem - Before MemClr	0xE04D
ABL Mem - Before On DIMM Thermal	0xE04E
ABL Mem - Before DMI	0xE04F
ABL MEM - End of phase 3 memory code	0xE050

5-10-5 CPU test points

Entry point CPU init after training	0xE051
Exit point CPU init after training	0xE052
Entry point CPU APOB CCX map init	0xE053
Exit point CPU APOB CCX map init	0xE054
Entry point CPU Optimized boot init	0xE055
Exit point CPU Optimized boot init	0xE056
Entry point CPU APOB EDC info init	0xE057
Exit point CPU APOB EDC info init	0xE058

5-10-6 Topology test points

ProcTopologyEntry	0xE071
ProcTopologyDone	0xE07C

5-10-7 Extended memory test point

ProcMemSendMRS2	0xE080
Sedding MRS3	0xE081
Sending MRS1	0xE082
Sending MRS0	0xE083
Continuous Pattern Read	0xE084
Continuous Pattern Write	0xE085
Mem: 2d RdDqs Training begin	0xE086
Mem: Before optional callout to platform BIOS to change External Vref during 2d Training	0xE087
Mem: After optional callout to platform BIOS to change External Vref during 2d Training	0xE088
Configure DCT For General use begin	0xE089
Configure DCT For training begin	0xE08A
Configure DCT For Non-Explicit	0xE08B
Configure to Sync channels	0xE08C
Allocate C6 Storage	0xE08D
Before LV DDR4	0xE08E
Before LV DDR3	0xE08F

5-10-8 Gnb Earlier init

TP0x90	0xE090
GNB earlier interface	0xE091
GNB internal debug code	0xE092
GNB internal debug code	0xE093
GNB internal debug code	0xE094
GNB internal debug code	0xE095
GNB internal debug code	0xE096
GNB internal debug code	0xE097
GNB internal debug code	0xE098
GNB internal debug code	0xE099
GNB internal debug code	0xE09A
GNB internal debug code	0xE09B
GNB internal debug code	0xE09C
GNB internal debug code	0xE09D
GNB internal debug code	0xE09E
GNB internal debug code	0xE09F
TP0xA0	0xE0A0
GNB internal debug code	0xE0A1
GNB internal debug code	0xE0A2
GNB internal debug code	0xE0A3
GNB internal debug code	0xE0A4
GNB internal debug code	0xE0A5
GNB internal debug code	0xE0A6
GNB internal debug code	0xE0A7
GNB internal debug code	0xE0A8
GNB internal debug code	0xE0A9
GNB internal debug code	0xE0AA
GNB internal debug code	0xE0AB
GNB internal debug code	0xE0AC
GNB internal debug code	0xE0AD
GNB internal debug code	0xE0AE
GNB internal debug code	0xE0AF
ABL 1 Begin	0xE0B0
ABL 1 Initialization	0xE0B1
ABL 1 DF Early	0xE0B2
ABL 1 DF Pre Training	0xE0B3
ABL 1 Debug Synchronization	0xE0B4
ABL 1 Error Detected	0xE0B5
ABL 1 Global memory error detected	0xE0B6
ABL 1 End	0xE0B7

ABL 2 Begin	0xE0B8
ABL 2 Initialization	0xE0B9
ABL 2 After Training	0xE0BA
ABL 2 Debug Synchronization	0xE0BB
ABL 2 Error detected	0xE0BC
ABL 2 Global memory error detected	0xE0BD
ABL 2 End	0xE0BE
ABL 3 Begin	0xE0BF
ABL 3 Initialziation	0xE0C0
ABL 3 GMI/xGMI Initialization Stage 1	0xB1C0
ABL 3 GMI/xGMI Initialization Stage 1 Warning	0xF1C0
ABL 3 GMI/xGMI Initialization Stage 2 Error	0xE2C0
ABL 3 GMI/xGMI Initialization Stage 2	0xB2C0
ABL 3 GMI/xGMI Initialization Stage 2 Warning	0xF2C0
ABL 3 GMI/xGMI Initialization Stage 2 Error	0xE3C0
ABL 3 GMI/xGMI Initialization Stage 3	0xB3C0
ABL 3 GMI/xGMI Initialization Stage 3 Warning	0xF3C0
ABL 3 GMI/xGMI Initialization Stage 3 Error	0xE4C0
ABL 3 GMI/xGMI Initialization Stage 4	0xB4C0
ABL 3 GMI/xGMI Initialization Stage 4 Warning	0xF4C0
ABL 3 GMI/xGMI Initialization Stage 4 Error	0xE5C0
ABL 3 GMI/xGMI Initialization Stage 5	0xB5C0
ABL 3 GMI/xGMI Initialization Stage 5 Warning	0xF5C0
ABL 3 GMI/xGMI Initialization Stage 5 Error	0xE6C0
ABL 3 GMI/xGMI Initialization Stage 6	0xB6C0
ABL 3 GMI/xGMI Initialization Stage 6 Warning	0xF6C0
ABL 3 GMI/xGMI Initialization Stage 6 Error	0xE7C0
ABL 3 GMI/xGMI Initialization Stage 7	0xE8C0
ABL 3 GMI/xGMI Initialization Stage 8	0xE9C0
ABL 3 GMI/xGMI Initialization Stage 9	0xF9C0
ABL 3 GMI/xGMI Initialization Stage 9 Error	0xEAC0
ABL 3 GMI/xGMI Initialization Stage 10	0xFAC0
ABL 3 GMI/xGMI Initialization Stage 10 Error	0xE0C1
ABL 3 ProgramUmcKeys	0xE0C2
ABL 3 DF Finial Initalization	0xE0C3
ABL 3 Execute Synchronization Function	0xE0C4
ABL 3 Debug Synchronization Function	0xE0C5
ABL 3 Error Detected	0xE0C6
ABL 3 Global memory error detected	0xE0C7
ABL 4 Initialization - cold boot	0xE0C8
ABL 4 Memory test - cold boot	0xE0C9

ABL 4 APOB Initialization - cold boot	0xE0CA
ABL 4 Finalize memory settings - cold boot	0xE0CB
ABL 4 CPU Initialize Optimized Boot - cold boot	0xE0CC
ABL 4 Gmi Pcie Training - cold boot	0xE0CD
ABL 4 Cold boot End	0xE0CE
ABL 4 Initialization - Resume boot	0xE0CF
ABL 4 Resume End	0xE0D0
ABL 4 End Cold/Resume boot	0xE0D1
ABL 2 memory initialization	0xE0D2
ABL 3 memory initialization	0xE0D3
ABL 3 End	0xE0D4
ABL 1 Enter Memory Flow	0xE0D5
Memory flow memory clock synchronization	0xE0D6
IfAmdReadEventLogEntry	0xE0D7
Exiting from AmdReadEventLog	0xE0D8
Entry to AmdGetApicId	0xE0D9
Exiting from AmdGetApicId	0xE0DA
Entry to AmdGetPciAddress	0xE0DB
Exiting from AmdGetPciAddress	0xE0DC
Entry to AmdIdentifyCore	0xE0DD
TExiting from AmdIdentifyCore	0xE0DE
After IDS calls out to run code on an AP	0xE0DF
After IDS calls out to run code on an AP	0xE0E0
Before IDS calls out to get IDS data	0xE0E1
After IDS calls out to get IDS data	0xE0E2
Before the heap manager calls out to allocate a buffer	0xE0E3
After the heap manager calls out to allocate a buffer	0xE0E4
Before the heap manager calls out to deallocate a buffer	0xE0E5
After the heap manager calls out to deallocate a buffer	0xE0E6
Before the heap manager calls out to locate a buffer	0xE0E7
After the heap manager calls out to locate a buffer	0xE0E8
Memory flow P-State synchronization	0xE0E9
After the BSP calls out to run code on an AP	0xE0EA
Before the BSP calls out to run code on an AP	0xE0EB
After the BSP calls out to run code on an AP	0xE0EC
Before the S3 save code calls out to allocate a buffer	0xE0ED
After the S3 save code calls out to allocate a buffer	0xE0EE
Before the memory S3 save code calls out to allocate a buffer	0xE0EF
After the memory S3 save code calls out to allocate a buffer	0xE0F0
Before the memory code calls out to locate a buffer	0xE0F1
After the memory code calls out to locate a buffer	0xE0F2

Before the memory code calls out to locate a buffer	0xE0F3
After the memory code calls out to locate a buffer	0xE0F4
Before the memory code calls out to locate a buffer	0xE0F5
After the memory code calls out to locate a buffer	0xE0F6
Before the memory code calls out to locate a buffer	0xE0F7
After the memory code calls out to locate a buffer	0xE0F8
Ready to boot event	

5-10-9 PMU test points

Failed PMU training	0xE0F9
End of phase 1 memory code	0xE0FA
End of phase 2 memory code	0xE0FB

5-10-10 ABL0 test points

Abl0Begin	0xE0FC
ABL 0 End	0xE0FD

5-10-11 ABL5 test points

ABL 5 End	0xE100
sume boot	0xE101
ABL 6 End	0xE102
ABL 6 Initialization	0xE103
End of phase 1b memory code	0xE104
ABL 1b memory initialization	0xE105
ABL 6 Global memroy error detected	0xE106
ABL 1b Debug Synchronization Function	0xE107
ABL 4b Debug Synchronization Function	0xE108
AblbBegin	0xE109
Ab4bBegin	0xE10A
BSP encountered HMAC fail on APOB Header	0xE10B
ABL Eroor General ASSERT	0xE2A0
Unknown Error	0xE2A1
ABL Error Log Inig Error	0xE2A2
ABL Error for On DIMM thermal Heap allocation error	0xE2A3
ABL Error for memory test error	0xE2A4
ABL Error while executing memory test error	0xE2A5
ABL Error DDR Post Packge Repair Mem Auto Heap Alloc error	0xE2A6
ABL Error for DDR Post Package repair Apob Heap Alloc error	0xE2A7
ABL Error for DDR Post Package Repair No PPR Table Heap Aloc error	0xE2A8
ABL Error for Ecc Mem Auto Aloc Error error	0xE2A9
ABL Error for Soc Scan Heap Aloc error	0xE2AB

ABL Error for Soc Scan No Die error	0xE2AC
ABL Error for Nb Tech Heap Aloc error	0xE2AD
ABL Error for No Nb Constructor error	0xE2AE
ABL Error for No Tech Constructor error	0xE2AE
ABL Error for ABL1b Auto Alocation error	0xE2B0
ABL Error for ABL1b No NB Constructor error	0xE2B1
ABL Error for ABL2 No Nb Constructor error	0xE2B2
ABL Error for ABL3 Auto Allocation error	0xE2B3
ABL Error for ABL3 No Nb Constructor error	0xE2B4
ABL Error for ABL1b General error	0xE2B5
ABL Error for ABL2 General error	0xE2B6
ABL Error for ABL3 General error	0xE2B7
ABL Error for Get Target Speed error	0xE2B8
ABL Error for Flow P1 Family Support error	0xE2B9
ABL Error for No Valid Ddr4 Dimms error	0xE2BA
ABL Error for No Dimm Present error	0xE2BB
ABL Error for Flow P2 Family Supprot error	0xE2BC
ABL Error for Heap Deallocation for PMU Sram Msg Block error	0xE2BD
ABL Error for DDR Recovery error	0xE2BE
ABL Error for RRW Test error	0xE2BF
ABL Error for On Die Thermal error	0xE2C1
ABL Error for Heap Allocation For Dct Struct Amd Ch Def structure error	0xE2C2
ABL Error for Heap Allocation for PMU SRAM Msg block error	0xE2C3
ABL Error for Heap Phy PLL lock Flure error	0xE2C4
ABL Error for Pmu Training error	0xE2C5
ABL Error for Failure to Load or Verify PMU FW error	0xE2C6
ABL Error for Allocate for PMU SRAM Msg Block No Init error	0xE2C7
ABL Error for Failure BIOS PMU FW Mismatch AGESA PMU FW version error	0xE2C8
ABL Error for Deallocate for PMU SRAM Msg Block error	0xE2CA
ABL Error for Module Type Mismatch RDIMM error	0xE2CB
ABL Error for Module type Mismatch LRDIMM error	0xE2CC
ABL Error for MEm Auto NVDIM error	0xE2CD
ABL Error for Unknowm Responce error	0xE2CE
ABL Error for Over Clock Error RRW Test Results Error	0xE2CF
ABL Error for Over Clock Error PMU Training Error	0xE2D0
ABL Error for ABL1 General Error	0xE2D1
ABL Error for ABL2 General Error	0xE2D2
ABL Error for ABL3 General Error	0xE2D3
ABL Error for ABL4 General Error	0xE2D4

ABL Error over clock Mem Init Error	0xE2D5
ABL Error over clock Mem Other Error	0xE2D6
ABL Error for ABL6 General Error	0xE2D7
ABL Error Event Log Error	0xE2D8
ABL Error FATAL ABL1 Log Error	0xE2D9
ABL Error FATAL ABL2 Log Error	0xE2DA
ABL Error FATAL ABL3 Log Error	0xE2DB
ABL Error FATAL ABL4 Log Error	0xE2DC
ABL Error Slave Sync function execution Error	0xE2DD
ABL Error Slave Sync communicaton with data set to master Error	0xE2DE
ABL Error Slave broadcast communication from master to slave Error	0xE2DF
ABL Error FATAL ABL6 Log Error	0xE2E0
ABL Error Slave Offline Error	0xE2E1
ABL Error Slave Informs Master Error Info Error	0xE2E2
ABL Error Error Heap Locate for PMU SRAM Msg Block Error	0xE2E3
ABL Error ABL2 Auto Error	0xE2E4
ABL Error Flow P3 Family support Error	0xE2E5
ABL Error Abl 4 Gen Error	0xE2EB
ABL Error MBIST Heap Allocation Error	0xE2EC
ABL Error MBIST Results Error	0xE2EE
ABL Error NO Dimm Smcus Info Error	0xE2EE
ABL Error Por Max Freq Table Error	0xE2EF
ABL Error Unsupproted DIMM Config Error	0xE2F0
ABL Error No Ps Table Error	0xE2F1
ABL Error Cad Bus Timing Not Found Error	0xE2F2
ABL Error Data Bus Timing Not Found Error	0xE2F3
ABL Error LrDIMM IBT Not Found Error	0xE2F4
ABL Error Unsupprote Dimm Config Max Freq Error Error	0xE2F5
ABL Error Mr0 Not Found Error	0xE2F6
ABL Error Obt Pattern Not found Error	0xE2F7
ABL Error Rc10 Op Speed Not FOund Error	0xE2F8
ABL Error Rc2 Ibt Not Found Error	0xE2F9
ABL Error Rtt Not Found Error	0xE2FA
ABL Error Checksum ReStrt Results Error	0xE2FB
ABL Error No Chipselect Results Error	0xE2FC
ABL Error No Common Cas Latency Results Error	0xE2FD
ABL Error Cas Latecncy exceeds Taa Max Error	0xE2FE
ABL Error Nvdimm Arm Missmatch Power Policy Error	0xE2FF
ABL Error Nvdimm Arm Missmatch Power Source Error	0xE300
ABL Error ABL 1 Mem Init Error	0xE301

ABL Error ABL 2 Mem Init Error	0xE302
ABL Error ABL 4 Mem Init Error	0xE303
ABL Error ABL 6 Mem Init Error	0xE304
ABL Error ABL 1 error repor Error	0xE305
ABL Error ABL 2 error repor Error	0xE306
ABL Error ABL 3 error repor Error	0xE307
ABL Error ABL 4 error repor Error	0xE308
ABL Error ABL 6 error repor Error	0xE30A
ABL Error message slave sync function execution Error	0xE30B
ABL Error slave offline Error	0xE30C
ABL Error Sync Master Error	0xE30D
ABL Error Slave Informs Master Info Message Error	0xE30E
ABL Error General Assert Error	0xE30F
ABL Error No Dimms On Any Channel in sysem	0xE310
ABL Alert PMU Major Message captured	0xE311
ABL Alert PMU REsults Rx Timing captured	0xE312
ABL Alert PMU REsults Tx Timing captured	0xE313
ABL Alert PMU REsults Rx Vref captured	0xE314
ABL Alert PMU REsults Tx Vref captured	0xE315
EndAgesas	0xEFFF

5-11 Agesa POST Codes

5-11-1 Universal Post Code

Universal ACPI entry	0xA001
Universal ACPI exit	0xA002
Universal ACPI abort	0xA003
Universal SMBIOS entry	0xA004
Universal SMBIOS exit	0xA005
Universal SMBIOS abort	0xA006

5-11-2 [0xA1XX] For CZ only memory Postcodes

Memory structure initialization (Public interface)	0xA101
SPD Data processing (Public interface)	0xA102
Memory configuration (Public interface)	0xA103
DRAM initialization	0xA104
TpProcMemSPDChecking	0xA105
TpProcMemModeChecking	0xA106
Speed and TCL configuration	0xA107
TpProcMemSpdTiming	0xA108
TpProcMemDramMapping	0xA109
TpProcMemPlatformSpecificConfig	0xA10A
TPProcMemPhyCompensation	0xA10B
TpProcMemStartDcts	0xA10C
(Public interface)	0xA10D
TpProcMemPhyFenceTraining	0xA10E
TpProcMemSynchronizeDcts	0xA10F
TpProcMemSystemMemoryMapping	0xA110
TpProcMemMtrrConfiguration	0xA111
TpProcMemDramTraining	0xA112
(Public interface)	0xA113
TpProcMemWriteLevelizationTraining	0xA114
Below 800Mhz first pass start	0xA115
Above 800Mhz second pass start	0xA116
Target DIMM configured	0xA117
Prepare DIMMS for WL	0xA118
Configure DIMMS for WL	0xA119
TpProcMemReceiverEnableTraining	0xA11A
Start sweep loop	0xA11B
Set receiver Delay	0xA11C
Write test pattern	0xA11D
Read test pattern	0xA11E
Compare test pattern	0xA11F

Calculate MaxRdLatency per channel	0xA120
TpProcMemReceiveDqsTraining	0xA121
Set Write Data delay	0xA122
Write test pattern	0xA123
Start read sweep	0xA124
Set Receive DQS delay	0xA125
Read Test pattern	0xA126
Compare Test pattern	0xA127
Update results	0xA128
Start Find passing window	0xA129
TpProcMemTransmitDqsTraining	0xA12A
Start write sweep	0xA12B
Set Transmit DQ delay	0xA12C
Write test pattern	0xA12D
Read Test pattern	0xA12E
Compare Test pattern	0xA12F
Update results	0xA130
Start Find passing window	0xA131
TpProcMemMaxRdLatencyTraining	0xA132
Start sweep	0xA133
Set delay	0xA134
Write test pattern	0xA135
Read Test pattern	0xA136
Compare Test pattern	0xA137
Online Spare init	0xA138
Bank Interleave Init	0xA139
Node Interleave Init	0xA13A
Channel Interleave Init	0xA13B
ECC initialization	0xA13C
Platform Specific Init	0xA13D
Before callout for "AgesaReadSpd"	0xA13E
After callout for "AgesaReadSpd"	0xA13F
Before optional callout "AgesaHookBeforeDramInit"	0xA140
After optional callout "AgesaHookBeforeDramInit"	0xA141
Before optional callout "AgesaHookBeforeDQSTraining"	0xA142
After optional callout "AgesaHookBeforeDQSTraining"	0xA143
Before optional callout "AgesaHookBeforeDramInit"	0xA144
After optional callout "AgesaHookBeforeDramInit"	0xA145
After MemDataInit	0xA146
Before InitializeMCT	0xA147
Before LV DDR3	0xA148

Before InitMCT	0xA149
Before OtherTiming	0xA14A
Before UMAMemTyping	0xA14B
Before SetDqsEccTmgs	0xA14C
Before MemClr	0xA14D
Before On DIMM Thermal	0xA14E
Before DMI	0xA14F
End of memory code	0xA150
Entry point S3Init	0xA151
Sending MRS2	0xA180
Sedding MRS3	0xA181
Sending MRS1	0xA182
Sending MRS0	0xA183
Continuous Pattern Read	0xA184
Continuous Pattern Write	0xA185
Mem: 2d RdDqs Training begin	0xA186
Mem: Before optional callout to platform BIOS to change External Vref during 2d Training	0xA187
Mem: After optional callout to platform BIOS to change External Vref during 2d Training	0xA188
Configure DCT For General use begin	0xA189
Configure DCT For training begin	0xA18A
Configure DCT For Non-Explicit	0xA18B
Configure to Sync channels	0xA18C
Allocate C6 Storage	0xA18D
Before LV DDR4	0xA18E
// BR CPU	
BR before AP launch	0xA190
Install AP launched PPI	0xA191
BR after AP launch	0xA192
Before CPU PM	0xA193
Enable IO Cstate	0xA194
Enable C6	0xA195
Install CCX PEI complete PPI	0xA196
BR CPU memory done call back entry	0xA197
Before APM weights	0xA198
After APM weights	0xA199
BR CPU memory done call back end	0xA19A
BR Init Mid entry	0xA19B
BR enable APM	0xA19C
BR Init Mid install protocol	0xA19D

BR Init Mid end	0xA19E
BR Init Late entry	0xA19F
BR Init Late install protocol	0xA1A0
BR Init Late end	0xA1A1
BR DXE install complete protocol	0xA1A2
UNB install complete PPI	0xA1A3
UNB AfterApLaunch callback entry	0xA1A4
UNB AfterApLaunch callback end	0xA1A5

5-11-3 S3 Interface Post Code

Before the S3 save code calls out to allocate a buffer	0xA1EC
After the S3 save code calls out to allocate a buffer	0xA1ED
Before the memory S3 save code calls out to allocate a buffer	0xA1EE
After the memory S3 save code calls out to allocate a buffer	0xA1EF
Before the memory code calls out to locate a buffer	0xA1F0
After the memory code calls out to locate a buffer	0xA1F1
Before the memory code calls out to locate a buffer	0xA1F2
After the memory code calls out to locate a buffer	0xA1F3
Before the memory code calls out to locate a buffer	0xA1F4
After the memory code calls out to locate a buffer	0xA1F5
Before the memory code calls out to locate a buffer	0xA1F6
After the memory code calls out to locate a buffer	0xA1F7

5-11-4 PMU Post Code

Failed PMU training	0xA1F9

5-11-5 [0xA5XX] assigned for AGESA PSP Module

// PSP V1 Modules	
PspPeiV1 entry	0xA501
PspPeiV1 exit	0xA502
MemoryDiscoveredPpiCallback entry	0xA503
MemoryDiscoveredPpiCallback exit	0xA504
PspDxeV1 entry	0xA507
PspDxeV1 exit	0xA508
PspDxeV1 PspPciEnumerationCompleteCallBack entry	0xA50A
PspDxeV1 PspPciEnumerationCompleteCallBack exit	0xA50B
PspDxeV1 ready to boot entry	0xA50C
PspDxeV1 ready to boot exit	0xA50D
PspSmmV1 entry	0xA50E
PspSmmV1 exit	0xA50F
PspSmmV1 SwSmiCallBack entry, build the S3 save area for resume	0xA510

PspSmmV1 SwSmiCallBack exit, build the S3 save area for resume	0xA511
PspSmmV1 BspSmmResumeVector entry	0xA512
PspSmmV1 BspSmmResumeVector exit	0xA513
PspSmmV1 ApSmmResumeVector entry	0xA514
PspSmmV1 ApSmmResumeVector exit	0xA515
PspP2CmboxV1 entry	0xA516
PspP2CmboxV1 exit	0xA517
// PSP V2 Modules	
PspPeiV2 entry	0xA521
PspPeiV2 exit	0xA522
PspDxeV2 entry	0xA523
PspDxeV2 exit	0xA524
PspDxeV2 PspMpServiceCallBack entry	0xA525
PspDxeV2 PspMpServiceCallBack exit	0xA526
PspDxeV2 FlashAccCallBack entry	0xA527
PspDxeV2 FlashAccCallBack exit	0xA528
PspDxeV2 ready to boot entry	0xA529
PspDxeV2 ready to boot exit	0xA52A
PspDxeV2 exit boot serivce entry	0xA52B
PspDxeV2 exit boot serivce exit	0xA52C
PspSmmV2 entry	0xA52D
PspSmmV2 exit	0xA52E
PspSmmV2 SwSmiCallBack entry, build the S3 save area for resume	0xA52F
PspSmmV2 SwSmiCallBack exit, build the S3 save area for resume	0xA530
PspSmmV2 BspSmmResumeVector entry	0xA531
PspSmmV2 BspSmmResumeVector exit	0xA532
PspSmmV2 ApSmmResumeVector entry	0xA533
PspSmmV2 ApSmmResumeVector exit	0xA534
PspP2CmboxV2 entry	0xA535
PspP2CmboxV2 exit	0xA536
TpPspRecoverApcbFail	0xA537
// PSP fTpm modules	
PspfTpmPei entry	0xA540
PspfTpmPei exit	0xA541
PspfTpmPei memory callback entry	0xA542
PspfTpmPei memory callback exit	0xA543
PspfTpmDxe entry	0xA544
PspfTpmDxe exit	0xA545
// P2C mailbox Handling [0xA59X]	
PspP2Cmbox Command SpiGetAttrib Handling entry	0xA591

PspP2Cmbox Command SpiSetAttrib Handling entry	0xA592
PspP2Cmbox Command SpiGetBlockSize Handling entry	0xA593
PspP2Cmbox Command SpiReadFV Handling entry	0xA594
PspP2Cmbox Command SpiWriteFV Handling entry	0xA595
PspP2Cmbox Command SpiEraseFV Handling entry	0xA596
PspP2Cmbox Command Handling exit	0xA59E
PspP2Cmbox Command Handling Fail exit	0xA59F
// C2P mailbox Handling	
PSP C2P mailbox entry base [0xA5BX | Cmd]	0xA5B0
Before send C2P command MboxBiosCmdDramInfo	0xA5B1
Before send C2P command MboxBiosCmdSmmInfo	0xA5B2
Before send C2P command MboxBiosCmdSleep SxInfo	0xA5B3
Before send C2P command MboxBiosCmdRsmInfo	0xA5B4
Before send C2P command MboxBiosCmdQueryCap	0xA5B5
Before send C2P command MboxBiosCmdBootDone	0xA5B6
Before send C2P command MboxBiosCmdClearS3Sts	0xA5B7
Before send C2P command MboxBiosCmdS3DataInfo	0xA5B8
Before send C2P command MboxBiosCmdNop	0xA5B9
Before send C2P command MboxBiosCmdHSTIQuery	0xA5C4
Before send C2P command MboxBiosCmdClrSmmLock	0xA5C7
Before send C2P command MboxBiosCmdPcieInfo	0xA5C8
Before send C2P command MboxBiosCmdGetVersion	0xA5C9
PSP C2P mailbox exit base [0xA5DX | Cmd]	0xA5D0
Wait C2P command MboxBiosCmdDramInfo finished	0xA5D1
Wait C2P command MboxBiosCmdSmmInfo finished	0xA5D2
Wait C2P command MboxBiosCmdSleep SxInfo finished	0xA5D3
Wait C2P command MboxBiosCmdRsmInfo finished	0xA5D4
Wait C2P command MboxBiosCmdQueryCap finished	0xA5D5
Wait C2P command MboxBiosCmdBootDone finished	0xA5D6
Wait C2P command MboxBiosCmdClearS3Sts finished	0xA5D7
Wait C2P command MboxBiosCmdS3DataInfo finished	0xA5D8
Wait C2P command MboxBiosCmdNop finished	0xA5D9
Wait C2P command MboxBiosCmdHSTIQuery finished	0xA5E4
Wait C2P command MboxBiosCmdClrSmmLock finished	0xA5C7
Wait C2P command MboxBiosCmdPcieInfo finished	0xA5C8
Wait C2P command MboxBiosCmdGetVersion finished	0xA5C9
// fTPM command Handling [0xA5FX]	
PspfTpm send TPM command entry	0xA5F0
PspfTpm send TPM command exit	0xA5F1
PspfTpm receive TPM command entry	0xA5F2
PspfTpm receive TPM command exit	0xA5F3

5-11-6 [0xA9XX, 0xAAXX] assigned for AGESA NBIO Module

// NbioBase	
AmdNbioBase PEIM driver entry	0xA900
AmdNbioBase PEIM driver exit	0xA901
AmdNbioBase DXE driver entry	0xA902
AmdNbioBase DXE driver exit	0xA903
// PCIe	
AmdNbioPcie PEIM driver entry	0xA904
AmdNbioPcie PEIM driver exit	0xA905
AmdNbioPcie DXE driver entry	0xA906
AmdNbioPcie DXE driver exit	0xA907
// GFX	
AmdNbioGfx PEIM driver entry	0xA908
AmdNbioGfx PEIM driver exit	0xA909
AmdNbioGfx DXE driver entry	0xA90A
AmdNbioGfx DXE driver exit	0xA90B
// IOMMU	
AmdNbioIommu DXE driver entry	0xA90C
AmdNbioIommu DXE driver exit	0xA90D
// ALIB	
AmdNbioALIB DXE driver entry	0xA90E
AmdNbioALIB DXE driver exit	0xA90F
// SMU	
AmdSmuV8 PEIM driver entry	0xA910
AmdSmuV8 PEIM driver exit	0xA911
AmdSmuV8 DXE driver entry	0xA912
AmdSmuV8 DXE driver exit	0xA913
AmdSmuV9 PEIM driver entry	0xA914
AmdSmuV9 PEIM driver exit	0xA915
AmdSmuV9 DXE driver entry	0xA916
AmdSmuV9 DXE driver exit	0xA917
AmdSmuV10 PEIM driver entry	0xA918
AmdSmuV10 PEIM driver exit	0xA919
AmdSmuV10 DXE driver entry	0xA91A
AmdSmuV10 DXE driver exit	0xA91B
// IOMMU PEIM	
AmdNbioIommu PEIM driver entry	0xA920
AmdNbioIommu PEIM driver exit	0xA921
// APCB DXE	
APCB DXE Entry	0xA922
APCB DXE Exit	0xA923

// APCB SMM	
APCB SMM Entry	0xA924
APCB SMM Exit	0xA925
// [0xA950, 0xA99F] NBIO PPI/PROTOCOL Callback	
NbioTopologyConfigureCallback entry	0xA950
NbioTopologyConfigureCallback exit	0xA951
MemoryConfigDoneCallbackPpi entry	0xA952
MemoryConfigDoneCallbackPpi exit	0xA953
DxioInitializationCallbackPpi entry	0xA954
DxioInitializationCallbackPpi exit	0xA955
DispatchSmuV9Callback entry	0xA956
DispatchSmuV9Callback exit	0xA957
DispatchSmuV10Callback entry	0xA958
DispatchSmuV10Callback exit	0xA959
AmdPcieMiscInit Event entry	0xA95A
AmdPcieMiscInit Event exit	0xA95B
NbioBaseHookReadyToBoot Event entry	0xA95C
NbioBaseHookReadyToBoot Event exit	0xA95D
NbioBaseHookPciIO Event entry	0xA95E
NbioBaseHookPciIO Event exit	0xA95F
// [0xA980, 0xA99F] BR GNB Task	
GnbEarlyInterfaceCZ entry	0xA970
GnbEarlyInterfaceCZ exit	0xA971
PcieConfigurationInit entry	0xA972
PcieConfigurationInit exit	0xA973
GnbEarlierInterfaceCZ entry	0xA974
GnbEarlierInterfaceCZ exit	0xA975
PcieEarlyInterfaceCZ entry	0xA976
PcieEarlyInterfaceCZ exit	0xA977
PciePostEarlyInterfaceCZ entry	0xA978
PciePostEarlyInterfaceCZ exit	0xA979
GfxConfigPostInterfaceCZ entry	0xA97A
GfxConfigPostInterfaceCZ exit	0xA97B
GfxPostInterfaceCZ entry	0xA97C
GfxPostInterfaceCZ exit	0xA97D
GnbPostInterfaceCZ entry	0xA97E
GnbPostInterfaceCZ exit	0xA97F
PciePostInterfaceCZ entry	0xA980
PciePostInterfaceCZ exit	0xA981
GnbEnvInterfaceCZ entry	0xA982
GnbEnvInterfaceCZ exit	0xA983

GfxConfigEnvInterface entry	0xA984
GfxConfigEnvInterface exit	0xA985
GfxEnvInterfaceCZ entry	0xA986
GfxEnvInterfaceCZ exit	0xA987
GfxMidInterfaceCZ entry	0xA988
GfxMidInterfaceCZ exit	0xA989
GfxIntInfoTableInterfaceCZ entry	0xA98A
GfxIntInfoTableInterfaceCZ exit	0xA98B
PcieMidInterfaceCZ entry	0xA98C
PcieMidInterfaceCZ exit	0xA98D
GnbMidInterfaceCZ entry	0xA98E
GnbMidInterfaceCZ exit	0xA98F
GnbSmuMidInterfaceCZ entry	0xA990
GnbSmuMidInterfaceCZ exit	0xA991
InvokeAmdInitLate entry	0xA992
InvokeAmdInitLate exit	0xA993
GnbSmuServiceRequestV8 entry	0xA994
GnbSmuServiceRequestV8 exit	0xA995

5-11-7 [0xACXX] assigned for AGESA CCX Module

CCX IDS IDS_HOOK_CCX_AFTER_AP_LAUNCH	0xAC10
CCX PEI entry	0xAC50
CCX downcore entry	0xAC51
CCX DXE entry	0xAC55
CCX MP service callback entry	0xAC56
CCX Read To Boot callback entry	0xAC57
CCX SMM entry	0xAC5D
CCX PEI start to launch APs for S3	0xAC70
CCX PEI end of launching APs for S3	0xAC71
CCX start to launch AP	0xAC90
CCX launch AP is ended	0xAC91
CCX launch AP abort	0xAC92
CCX MP service abort	0xAC93
CCX cac weights	0xAC94
CCX PEI exit	0xACE0
CCX downcore exit	0xACE1
CCX DXE exit	0xACE5
CCX MP service callback exit	0xACE6
CCX Read To Boot callback exit	0xACE7
CCX SMM exit	0xACED

5-11-8 [0xADXX] assigned for AGESA DF Module

DF PEI entry	0xAD50
DF DXE entry	0xAD55
DF Ready to Boot entry	0xAD56
DF PEI exit	0xADE0
DF DXE exit	0xADE5
DF Ready to Boot exit	0xADE6

5-11-9 [0xAFXX] assigned for AGESA FCH Module

FCH InitReset dispatch point	0xAF01
FCH InitEnv dispatch point	0xAF06
FCH InitMid dispatch point	0xAF07
FCH InitLate dispatch point	0xAF08
FCH InitS3Early dispatch point	0xAF0B
FCH InitS3Late dispatch point	0xAF0C
FCH InitS3Early dispatch finished	0xAF0D
FCH InitS3Late dispatch finished	0xAF0E
FCH Pei Entry	0xAF10
FCH Pei Exit	0xAF11
FCH MultiFch Pei Entry	0xAF12
FCH MultiFch Pei Exit	0xAF13
FCH Dxe Entry	0xAF14
FCH Dxe Exit	0xAF15
FCH MultiFch Dxe Entry	0xAF16
FCH MultiFch Dxe Exit	0xAF17
FCH Smm Entry	0xAF18
FCH Smm Exit	0xAF19
FCH Smm Dispatcher Entry	0xAF20
FCH Smm Dispatcher Exit	0xAF21
FCH InitReset HwAcpi	0xAF40
FCH InitReset AB Link	0xAF41
FCH InitReset LPC	0xAF42
FCH InitReset SPI	0xAF43
FCH InitReset eSPI	0xAF44
FCH InitReset SD	0xAF45
FCH InitReset eMMC	0xAF46
FCH InitReset SATA	0xAF47
FCH InitReset USB	0xAF48
FCH InitReset xGbE	0xAF49
FCH InitReset HwAcpiP	0xAF4F
FCH InitEnv HwAcpi	0xAF50

FCH InitEnv AB Link	0xAF51
FCH InitEnv LPC	0xAF52
FCH InitEnv SPI	0xAF53
FCH InitEnv eSPI	0xAF54
FCH InitEnv SD	0xAF55
FCH InitEnv eMMC	0xAF56
FCH InitEnv SATA	0xAF57
FCH InitEnv USB	0xAF58
FCH InitEnv xGbE	0xAF59
FCH InitEnv HwAcpiP	0xAF5F
FCH InitMid HwAcpi	0xAF60
FCH InitMid AB Link	0xAF61
FCH InitMid LPC	0xAF62
FCH InitMid SPI	0xAF63
FCH InitMid eSPI	0xAF64
FCH InitMid SD	0xAF65
FCH InitMid eMMC	0xAF66
FCH InitMid SATA	0xAF67
FCH InitMid USB	0xAF68
FCH InitMid xGbE	0xAF69
FCH InitLate HwAcpi	0xAF70
FCH InitLate AB Link	0xAF71
FCH InitLate LPC	0xAF72
FCH InitLate SPI	0xAF73
FCH InitLate eSPI	0xAF74
FCH InitLate SD	0xAF75
FCH InitLate eMMC	0xAF76
FCH InitLate SATA	0xAF77
FCH InitLate USB	0xAF78
FCH InitLate xGbE	0xAF79
End of TP range for FCH	0xAFFF
Last defined AGESA PCs	0xFFFF

5-12 BIOS POST Beep code (AMI standard)

5-12-1 PEI Beep Codes

# of Beeps	Description
1	Memory not Installed.
1	Memory was installed twice (InstallPeiMemory routine in PEI Core called twice)
2	Recovery started
3	DXEIPL was not found
3	DXE Core Firmware Volume was not found
4	Recovery failed
4	S3 Resume failed
7	Reset PPI is not available

5-12-2 DXE Beep Codes

# of Beeps	Description
1	Invalid password
4	Some of the Architectural Protocols are not available
5	No Console Output Devices are found
5	No Console Input Devices are found
6	Flash update is failed
7	Reset protocol is not available
8	Platform PCI resource requirements cannot be met